Altera JESD204B IP Core and TI DAC37J84 Hardware Checkout Report

2014-09-22

AN-719

The Altera JESD204B MegaCore function is a high-speed point-to-point serial interface intellectual property (IP).

The JESD204B IP core has been hardware-tested with a number of selected JESD204B-compliant ADC (analog-to-digital converter) and DAC (digital-to-analog) devices.

This report highlights the interoperability of the JESD204B IP core with the DAC37J84 converter evaluation module (EVM) from Texas Instruments Inc. (TI). The following sections describe the hardware checkout methodology and test results.

Hardware Requirements

The hardware checkout test requires the following hardware and software tools:

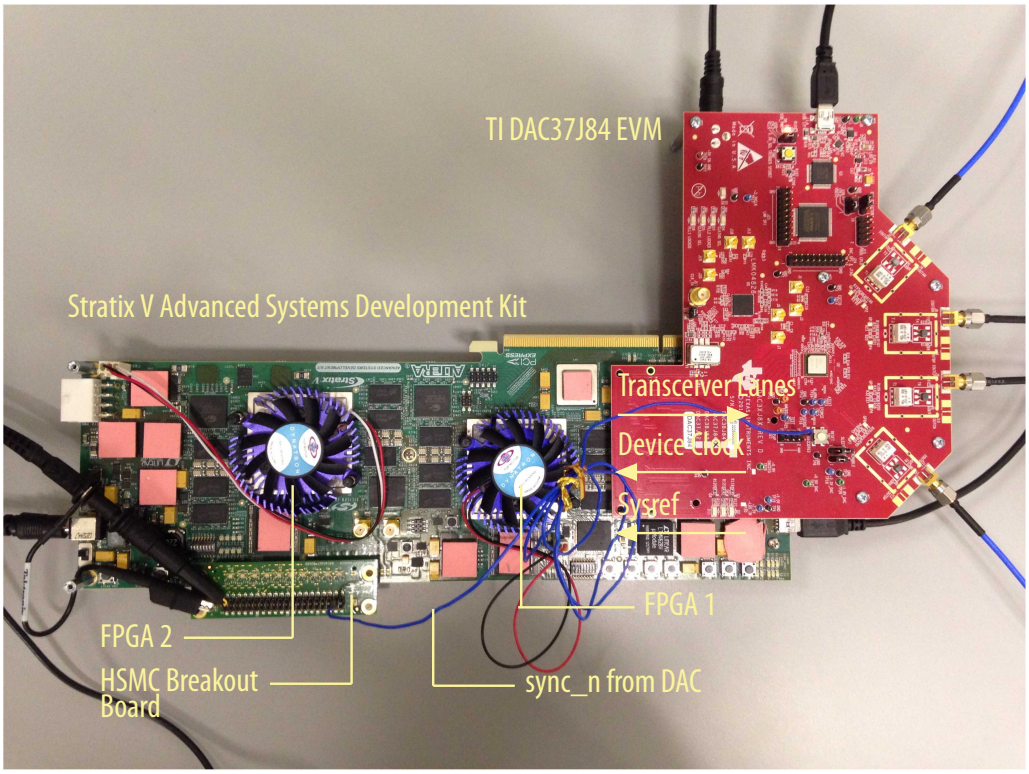
- Altera Stratix V Advanced Systems Development Kit with 15 V power adaptor
- HSMC breakout board included in the Stratix V Advanced Systems Development Kit
- TI DAC37J84 EVM with 5.0 V power adaptor
- Mini-USB cables
- SMA cables
- Wire for connecting J21 header to HSMC breakout board header
- Oscilloscope with a minimum bandwidth of 4 GHz

Hardware Setup

A Stratix V Advanced Systems Development Kit is used with the TI DAC37J84 daughter card module installed to the development board's FMC connector.

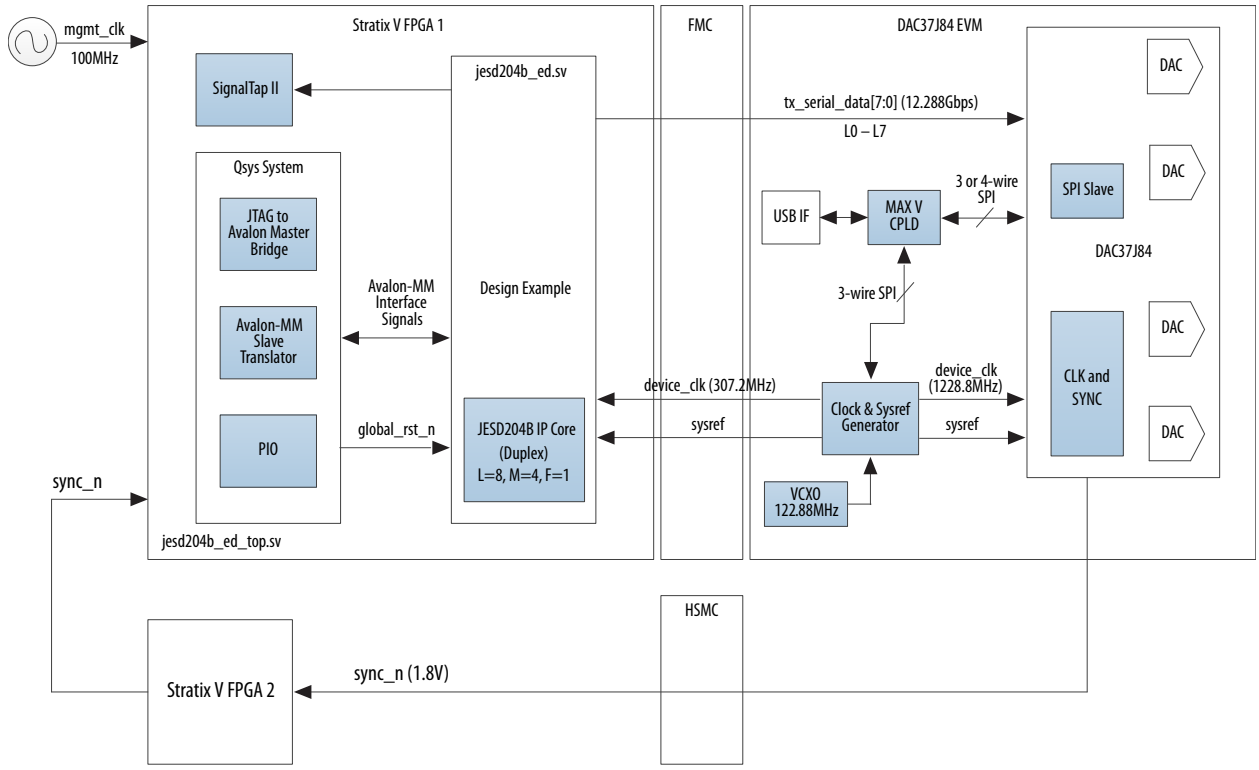
- The DAC37J84 EVM derives power from 5.0 V power adaptor.
- The FPGA and DAC device clock is supplied by the LMK04828 clock generator on the DAC37J84 EVM.
- For subclass 1, the LMK04828 clock generator generates *SYSREF* for the JESD204B IP core as well as the DAC37J84 device.
- The sync_n signal is transmitted from the DAC37J84 to FPGA through a wire connected to J21 (pin 1) of DAC37J84 EVM and HSMC breakout board (pin 3). (1)

Figure 1: Hardware Setup



(1) The sync_n signal from the DAC does not have direct connection to FPGA 1 through the FMC connector. The FPGA 2 is used as a bridge to transfer the sync_n signal to FPGA 1 through the HSMC connector.

Figure 2: System Diagram



The system-level diagram shows how the different modules connect in this design.

In this setup, where LMF = 841, the data rate of transceiver lanes is 12.288 Gbps. The LMK04828 clock generator provides 307.2 MHz device clock to the FPGA and 1228.8 MHz device clock to the DAC37J84 device. The LMK04828 provides *SYSREF* pulses to both the DAC and FPGA. A wire connects between J21 pin 1 on DAC37J84 EVM (SYNC_N_AB pin) and HSMC breakout board header pin 3 to transmit the sync_n signal from DAC37J84 to FPGA 2. The FPGA 2 acts as a passthrough to deliver sync_n signal to FPGA 1. The DAC37J84 operates in LINK0 only mode (single link) in all configurations.

Note: The FPGA 2 must be configured prior to connecting the wire that carries the sync_n signal to the HSMC breakout board header. Verify that the voltage at the targeted header pin is less than 1.8 V. Refer to the DAC37J84 datasheet for the absolute maximum rating of SYNC_N_AB pin.

DAC3XJ8XEVM Software Setup

The DAC3XJ8XEVM software configures the DAC37J84 device and LMK04828 clock generator for JESD204B link operation.

You need to configure the DAC and LMK04828 with the correct settings and sequence for the JESD204B link to operate at the targeted data rate and JESD204B link parameters. Follow these steps to set up the configuration via the DAC3XJ8XEVM graphical user interface (GUI):

1. Configure the FPGA.
2. In the **Quick Start** tab, select a value for **DAC Data Input Rate**, **Number of SerDes Lanes**, and **Interpolation** options to meet the settings as stated in **Table 6**. The DAC device clock is synonymous to the **DAC Output Rate**.
3. Click the **1. Program LMK04828 and DAC3XJ8X** button.
4. In the **DAC3XJ8X Controls** tab, select the **Clocking** sub tab. For the **SYNCing of Clock Dividers** drop-down list, select **Use all SYSREF pulses**.
5. In the **DAC3XJ8X Controls** tab, select the **JESD Block** sub tab.
   a. At the *Elastic Buffer* section, turn on the **Match Char.** checkbox.
   b. At the *Initialization Bits* section, turn off the **TX Does not allow lane syncing** checkbox.
   c. Change the K and RBD value accordingly. RBD value is K value minus 1. For example, when K = 32, set RBD = 31.
   d. At the *Configuration for All Lanes* section, for the **SCR** drop-down list, select **SCRAMBLE ON** if scrambler is turned on at the JESD204B IP core. Select **SCRAMBLE OFF** if scrambler is turned off at the JESD204B IP core.
   e. At the *Errors for SYNC Request and Reporting* section, under the **Link0 S** column, turn on the **Link configuration error**, **8b/10b not-in-table code error**, and **8b/10b disparity error** checkboxes. Optionally, you can turn off all the checkboxes under the **Link1 S R** columns.
6. In the **LMK04828 Controls** tab, select the **SYSREF and SYNC** sub tab.
   a. At the *FPGA Clock and SYSREF* section, turn on the **HS** checkbox for *DCLK Delay*.
   b. At the *SYSREF Configuration* section, change the **SYSREF Divider** value according to the mode and K value of the targeted operation:
      a. LMFS=148, K=16 and 32, SYSREF Divider=768
      b. LMFS=244, K=16 and 32, SYSREF Divider=512
      c. LMFS=4421, K=16 and 32, SYSREF Divider=256
      d. LMFS=8411, K=20, SYSREF Divider=80
      e. LMFS=8411, K=32, SYSREF Divider=128
   c. For the SYSREF Source drop-down list, select **Normal SYNC**.
   d. At the *SYNC Configuration* section, set the following:
      a. For the **SYNC Mode** drop-down list, select **Pin**.
      b. Turn off the **SYSREF SYNC Disable**, **DCLKout0 SYNC Disable**, and **DCLKout2 SYNC Disable** checkboxes.
      c. Turn on the **SYNC Pin Polarity** checkbox. Then turn off this option.
      d. Turn on the **SYSREF SYNC Disable**, **DCLKout0 SYNC Disable**, and **DCLKout2 SYNC Disable** checkboxes.
   e. At the *SYSREF Configuration* section, for the **SYSREF Source** drop-down list, select **SYSREF Pulses**.
7. In the **Quick Start** tab, click the **2. Reset DAC JESD Core** button. Then, click the **3. Trigger LMK04828 SYSREF** button

You can record steps 4 to 6 in a log file for future replay. Double-click the lower left corner (see Figure 3) of the software. A pop-up Status Log window is launched. Right click at the empty area and select "Clear Log" and close the pop-up window. Perform steps 4 to 6. Re-open the pop-up window and select the series of actions that are recorded. Right click at the empty area and save the selected actions into a file with .cfg extension. Use an editor to delete the read register records. Then transform the write register records into

the format as indicated in the sample setup files that are included in the graphical user interface (GUI) installation. A sample configuration file for the LMF=841, K=32, RBD=31, SCR=1 is shown below.

```
DAC3XJ8X
0x51 0x00FF //enable sync request for link 0
0x54 0x0000 //disable sync request for link 1
0x55 0x0000 //disable error reporting for link 1
0x4F 0x1CC1 //turn on lane sync, match specific character 0x1C to start JESD
buffering
0x4C 0x1F07 //K=32, L=8
0x4B 0x1E00 //RBD=31, F=1
0x4E 0x0F6F //SCR=1, HD=1
0x24 0x0010 //cdrvser_sysref_mode=use all sysref pulses

LMK04828
0x13A 0x00 //sysref divider=128
0x13B 0x80 //sysref divider=128
0x104 0x60 //half step for FPGA device clk
0x139 0x00 //set SYSREF_Mux to "Normal"
0x143 0x11 // trigger SYNC event using "Pin" mode
0x144 0x00 //enable syncing of all clock outputs
0x143 0x31 //toggle SYNC Pin Polarity bit
0x143 0x11 //toggle SYNC Pin Polarity bit
0x144 0xFF //disable syncing of all clock outputs
0x139 0x02 //set SYSREF_MUX to "Pulses"
```

The figures below show the examples of GUI setup for LMF = 841 configuration.

Figure 3: Quick Start Tab

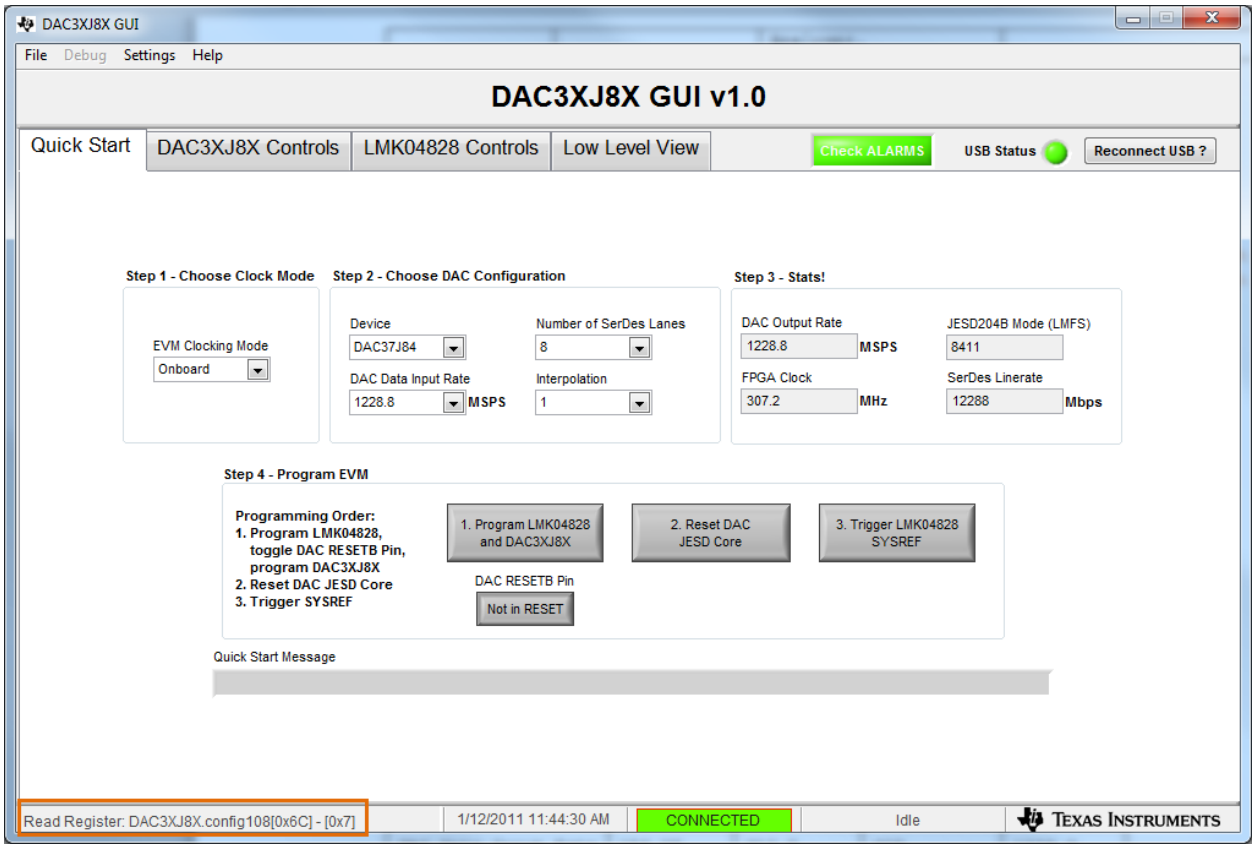


Figure 4: DAC3XJ8X Controls Tab - Clocking

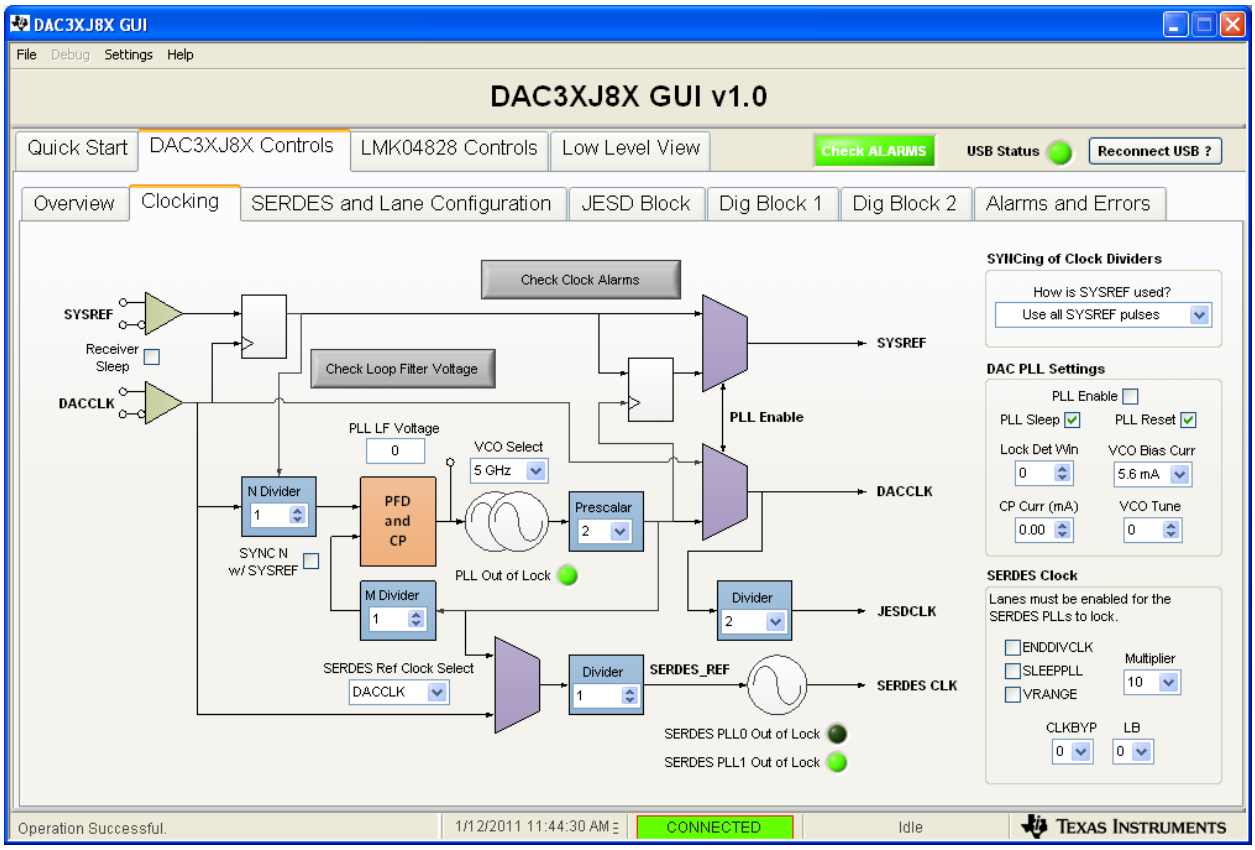


Figure 5: DAC3XJ8X Controls Tab - SERDES and Lane Configuration

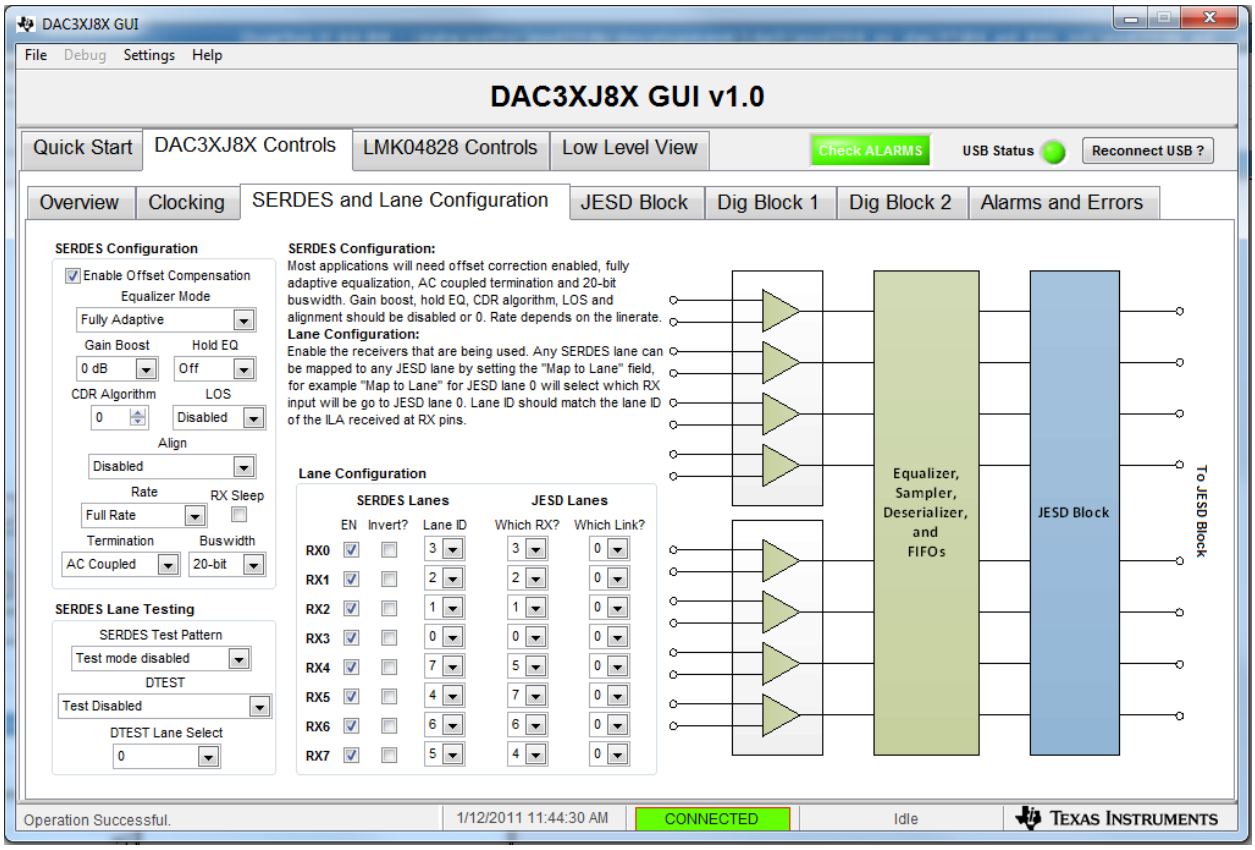


Figure 6: DAC3XJ8X Controls Tab - JESD Block

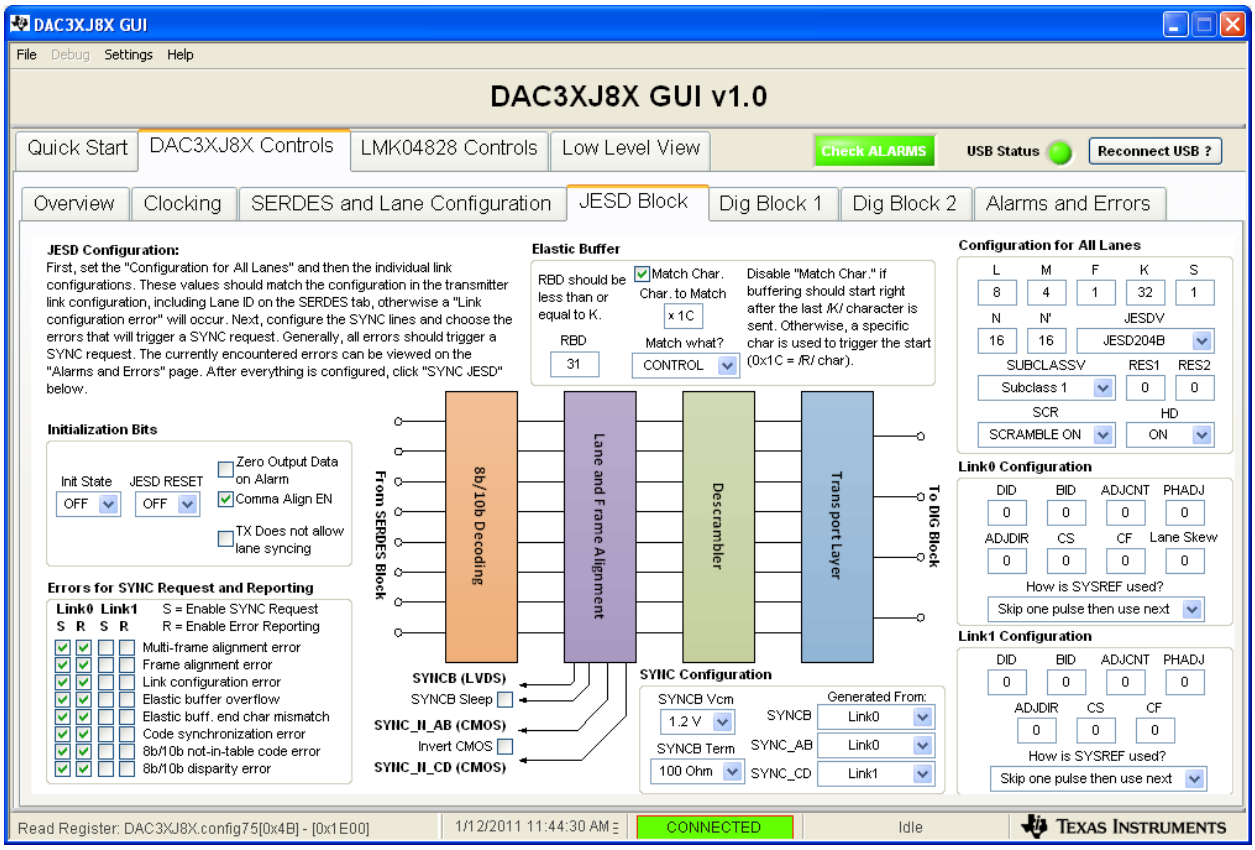


Figure 7: LMK04828 Controls Tab - SYSREF and SYNC

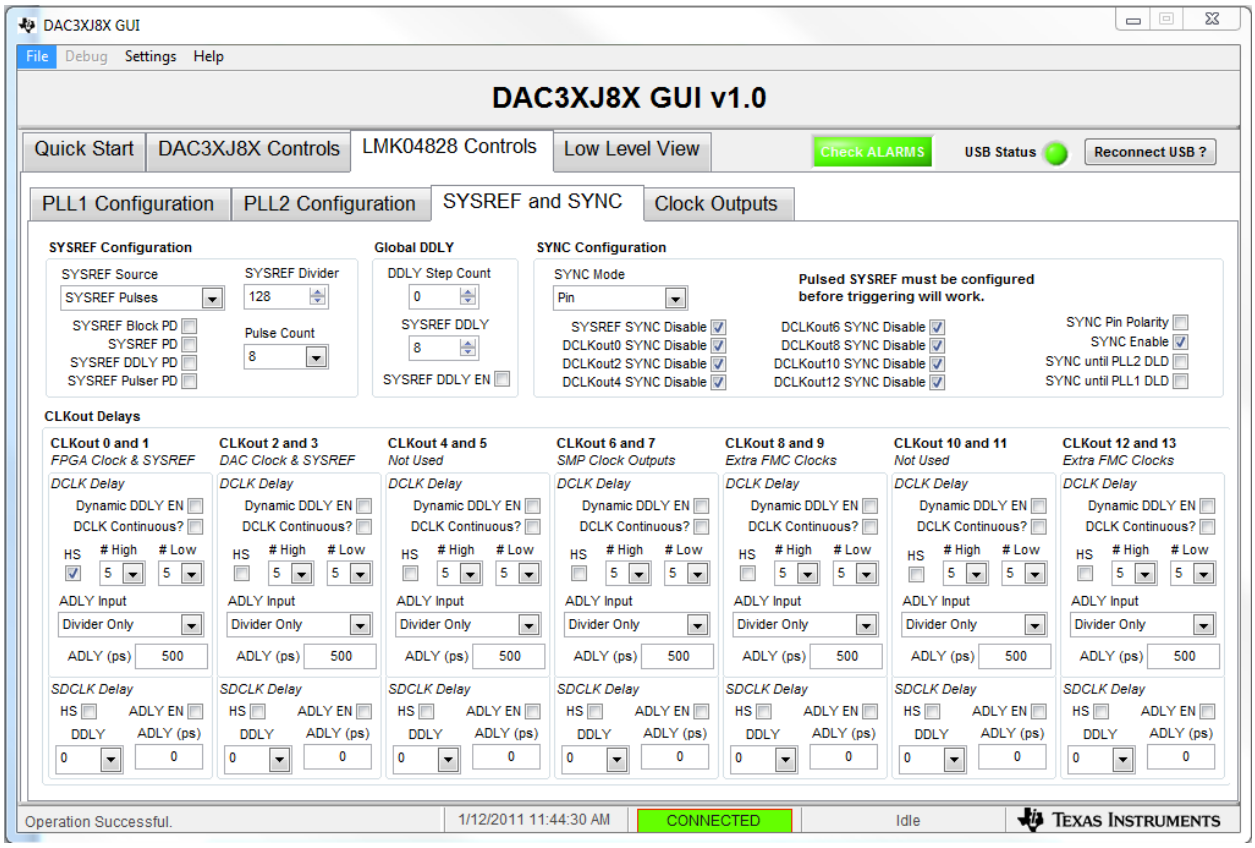
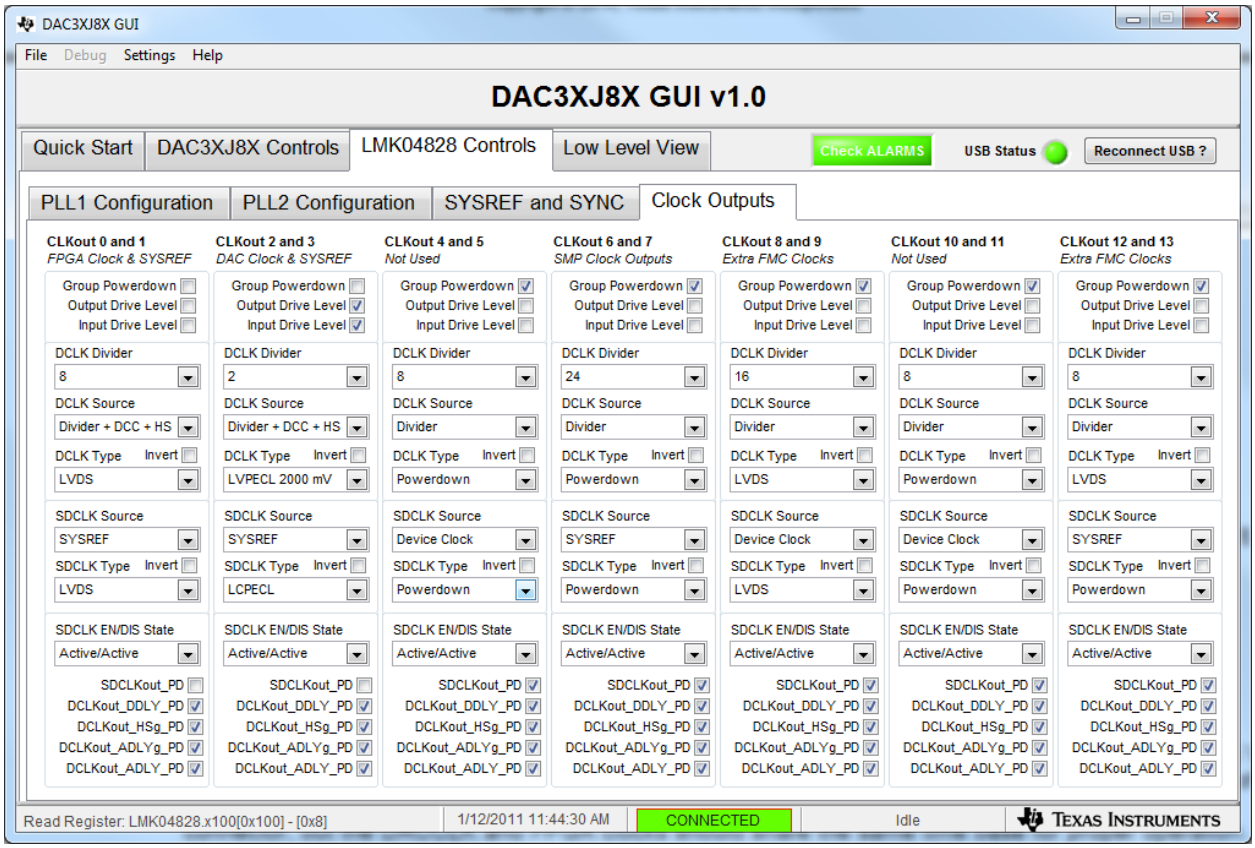


Figure 8: LMK04828 Controls Tab - Clock Outputs



The LMK04828 clocks:

- CLKout0 supplies device clock to the FPGA.
- CLKout1 is configured as the *SYSREF* source for the FPGA.
- CLKout2 supplies device clock to the DAC.
- CLKout3 is configured as the *SYSREF* source for the DAC.

To perform short transport layer test, you must properly set up the pattern checker at DAC transport layer according to the following steps:

1. Set bit 12 of the `config2` register (address 0x02) to enable short transport layer checker. To do this, highlight the `config2` register and check the bit 12 checkbox in the "DAC3XJ8X Controls > Low Level View" tab. Click the **Write Register** button to write the setting to the SPI interface of the DAC37J84.
2. Clear bits 8–15 of the `config6` register (address 0x06) to disable the "Short Test Error" alarm mask. Clear the bits according to the respective active lanes (for example, bit 8 is for lane0, bit 15 is for lane 7).

To do this, uncheck the **Short Test Error** checkboxes at the *Alarm Masking* section in the "DAC3XJ8X Controls > Alarms and Errors" tab.

3. Set the FPGA to output the corresponding test pattern, according to the parameter configuration listed in **Table 6**.
4. Check the result at bits 8–15 of the `config109` register. To do this, press the **Clear Alarms and Read** button in the "DAC3XJ8X Controls > Alarms and Errors" tab and monitor the **Short Test Error** indicator.

Figure 9: DAC3XJ8X Controls Tab - Alarms and Errors

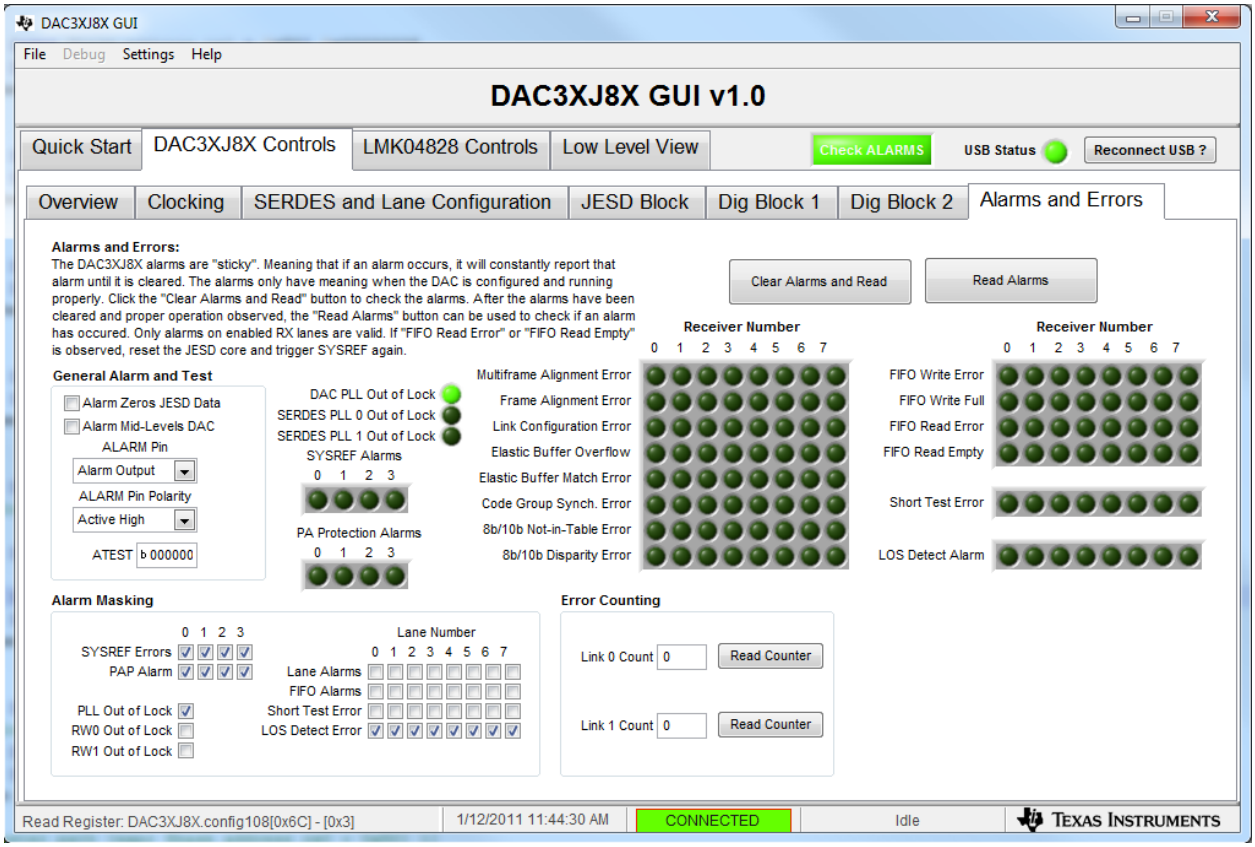
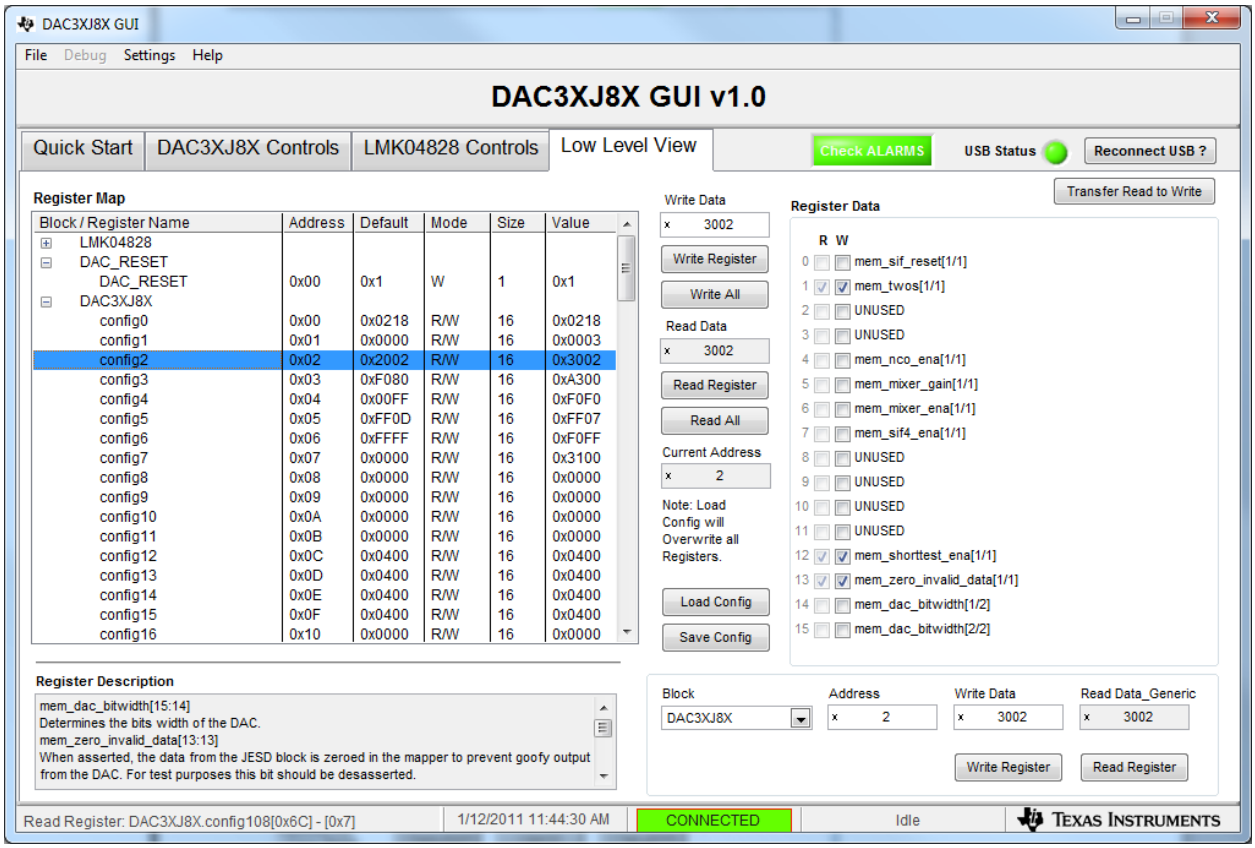


Figure 10: Low Level View Tab



Hardware Checkout Methodology

The following section describes the test objectives, procedure, and the passing criteria.

The hardware checkout test covers the following areas:

- Transmitter data link layer
- Transmitter transport layer
- Scrambling
- Deterministic latency (Subclass 1)

Transmitter Data Link Layer

This test area covers the test cases for code group synchronization (CGS) and initial lane alignment sequence (ILAS).

On link start up, the receiver issues a synchronization request and the transmitter transmits /K/ (K28.5) characters. The SignalTap II Logic Analyzer tool monitors the transmitter data link layer operation. The DAC3XJ8XEVM software GUI is used to monitor the receiver data link layer operation.

Code Group Synchronization (CGS)

Table 1: CGS Test Cases

Test Case	Objective	Description	Passing Criteria
CGS.1	Check that /K/ characters are transmitted when sync_n is asserted.	The following signals in <*ip_variant_name*>_inst_phy.v are tapped: • jesd204_tx_pcs_data[(L*32)-1:0] • jesd204_tx_pcs_kchar_data[(L*4)-1:0] (2) The following signals in <*ip_variant_name*>.v are tapped: • sync_n • jesd204_tx_int The txlink_clk is used as the SignalTap II sampling clock. Each lane is represented by 32-bit data bus in the jesd204_tx_pcs_data signal. The 32-bit data bus is divided into 4 octets. Check the following error in Alarm and Errors tab in the DAC3XJ8XEVM GUI: • Code Group Synch Error	• /K/ character or K28.5 (0xBC) is transmitted at each octet of the jesd204_tx_pcs_data bus when the receiver asserts the sync_n signal. • The jesd204_tx_pcs_kchar_data signal is asserted whenever control characters like /K/ characters are transmitted. • The jesd204_tx_int is deasserted if there is no error. • The "Code Group Synch Error" in GUI is not asserted.
CGS.2	Check that /K/ characters are transmitted after sync_n is deasserted but before the start of multiframe.	The following signals in <*ip_variant_name*>_inst_phy.v are tapped: • jesd204_tx_pcs_data[(L*32)-1:0] • jesd204_tx_pcs_kchar_data[(L*4)-1:0] (2) The following signals in <*ip_variant_name*>.v are tapped: • sync_n • tx_sysref • jesd204_tx_int The txlink_clk is used as the SignalTap II sampling clock. Each lane is represented by 32-bit data bus in the jesd204_tx_pcs_data signal. The 32-bit data bus is divided into 4 octets. Check the following error in Alarm and Errors tab in the DAC3XJ8XEVM GUI: • 8b/10b Not-in-Table Error • 8b/10b Disparity Error	• The /K/ character transmission continues for at least 1 frame plus 9 octets. • The sync_n and jesd204_tx_int signals are deasserted. • The "8b/10b Not-in-Table Error" and "8b/10b Disparity Error" in GUI are not asserted.

(2) L is the number of lanes.

Initial Lane Alignment Sequence (ILAS)

Table 2: ILAS Test Cases

Test Case	Objective	Description	Passing Criteria
ILA.1	Check that /R/ and /A/ characters are transmitted at the beginning and end of each multiframe. Verify that four multiframes are transmitted in ILAS phase and receiver detects the initial lane alignment sequence correctly.	The following signals in <*ip_variant_name*>_inst_phy.v are tapped: • jesd204_tx_pcs_data[(L*32)-1:0] • jesd204_rx_pcs_kchar_data[(L*4)-1:0] (3) The following signals in <*ip_variant_name*>.v are tapped: • sync_n • jesd204_tx_int The txlink_clk is used as the SignalTap II sampling clock. Each lane is represented by 32-bit data bus in the jesd204_tx_pcs_data signal. The 32-bit data bus is divided into 4 octets. Check the following error in "Alarm and Errors" tab in the DAC3XJ8XEVM GUI: • Frame Alignment Error • Multiframe Alignment Error	• The /R/ character or K28.0 (0x1C) is transmitted at the jesd204_tx_pcs_data bus to mark the beginning of multiframe. • The /A/ character or K28.3 (0x7C) is transmitted at the jesd204_tx_pcs_data bus to mark the end of each multiframe. • The sync_n and jesd204_tx_int signals are deasserted. • The jesd204_tx_pcs_kchar_data signal is asserted whenever control characters like /K/, /R/, /Q/ or /A/ characters are transmitted. • The "Frame Alignment Error" and "Multiframe Alignment Error" in the GUI are not asserted.

(3) L is the number of lanes.

Test Case	Objective	Description	Passing Criteria
ILA.2	Check the JESD204B configuration parameters are transmitted in the second multiframe.	The following signals in <*ip_variant_name*>_`inst_phy.v` are tapped: • jesd204_tx_pcs_data[(L*32)-1:0] (3) The following signal in <*ip_variant_name*>`.v` is tapped: • jesd204_tx_int The `txlink_clk` is used as the SignalTap II sampling clock. The system console accesses the following registers: • ilas_data0 • ilas_data1 • ilas_data2 • ilas_data4 • ilas_data5 The content of 14 configuration octets in the second multiframe is stored in these 32-bit registers - ilas_data0, ilas_data1, ilas_data2, ilas_data4 and ilas_data5. Check the following error in "Alarm and Errors" tab in the DAC3XJ8XEVM GUI: • Link Configuration Error	• The /R/ character is followed by /Q/ character or K28.4 (0x9C) in the `jesd204_tx_pcs_data` bus at the beginning of second multiframe. • The JESD204B parameters read from ilas_data0, ilas_data1, ilas_data2, ilas_data4, and ilas_data5 registers are the same as the parameters set in the JESD204B IP core Qsys parameter editor. • The `jesd204_tx_int` signal is deasserted if there is no error. • The "Link Configuration Error" in the GUI is not asserted.

Test Case	Objective	Description	Passing Criteria
ILA.3	Check the constant pattern of transmitted user data after the end of 4th multiframes. Verify that the receiver successfully enters user data phase.	The following signals in <*ip_variant_name*>_inst_phy.v are tapped: • jesd204_tx_pcs_data[(L*32)-1:0] The following signal in <*ip_variant_name*>.v is tapped: • jesd204_tx_int The txlink_clk is used as the SignalTap II sampling clock. The system console accesses the tx_err register. Check the following errors in the Alarm and Errors tab in the DAC3XJ8XEVM GUI: • Elastic Buffer Overflow • Elastic Buffer Match Error	• When scrambler is turned off, the first user data is transmitted after the last /A/ character, which marks the end of the 4th multiframe transmitted. (4) • The jesd204_tx_int signal is deasserted if there is no error. • Bits 2 and 3 of the tx_err register are not set to "1". • The "Elastic Buffer Overflow" and "Elastic Buffer Match Error" in the GUI are not asserted.

Transmitter Transport Layer

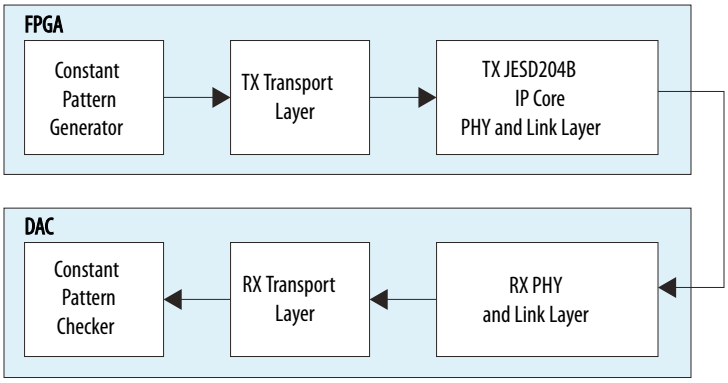
To verify the data integrity of the payload data stream through the TX JESD204B IP core and transport layer, the DAC JESD core is configured to check short transport layer test pattern that is transmitted from FPGA test pattern generator. The DAC JESD core checks the short transport layer test patterns based on F = 1, 2, 4 or 8 configuration. Refer to **Table 6** for the short transport layer test pattern configuration. The short test pattern has a duration of one frame period and is repeated continuously for the duration of the test.

To verify that data from the FPGA digital domain is successfully sent to the DAC analog domain, the FPGA is configured to generate a sine wave. Connect an oscilloscope to observe the waveform at the DAC analog channels.

(4) When scrambler is turned on, your data pattern cannot be recognized after the 4th multiframe in ILAS phase.

Figure 11: Data Integrity Check Using DAC Short Transport Layer Pattern Checker

This figure shows the conceptual test setup for short transport layer data integrity checking.



The SignalTap II Logic Analyzer tool monitors the operation of the TX transport layer.

Table 3: Transport Layer Test Cases

Test Case	Objective	Description	Passing Criteria
TL.1	Check the transport layer mapping using short transport layer test pattern as specified in the parameter configuration.	The following signals in `altera_jesd204_transport_tx_top.sv` are tapped: • jesd204_tx_data_valid • jesd204_tx_data_ready The following signal in `jesd204b_ed.sv` is tapped: • jesd204_tx_int The `txframe_clk` is used as the SignalTap II sampling clock. (5) Check the following error in "Alarm and Errors" tab in the DAC3XJ8XEVM GUI: • Short Test Error	• The `jesd204_tx_data_ready` and `jesd204_tx_data_valid` signals are asserted. • The "Short Test Error" is not asserted.
TL.2	Verify the data transfer from digital to analog domain.	Enable sine wave generator in the FPGA and observe the DAC analog channel output on the oscilloscope.	A monotone sine wave is observed on the oscilloscope.

(5) For LMF=148 configuration, the `txlink_clk` signal is used as the SignalTap II sampling clock as the `txlink_clk` frequency is two times of the `txframe_clk` frequency.

Scrambling

With descrambler enabled, the short transport layer test pattern checker at the DAC JESD core checks the data integrity of scrambler in the FPGA.

The SignalTap II Logic Analyzer tool monitors the operation of the TX transport layer.

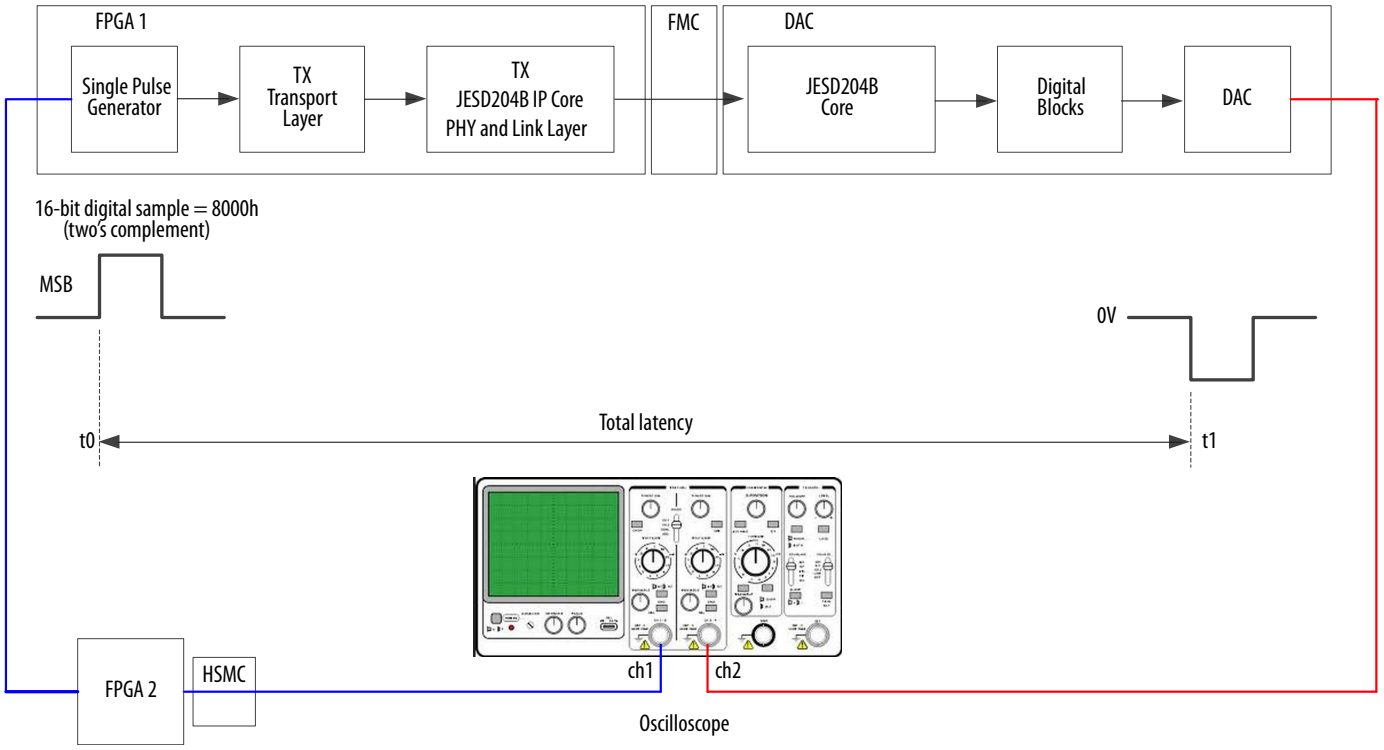
Table 4: Descrambler Test Cases

Test Case	Objective	Description	Passing Criteria
SCR.1	Check the functionality of the scrambler using short transport layer test pattern as specified in the parameter configuration.	Enable descrambler at the DAC JESD core and scrambler at the TX JESD204B IP core. The signals that are tapped in this test case are similar to test case TL.1 Check the following error in "Alarm and Errors" tab in the DAC3XJ8XEVM GUI: • Short Test Error	• The `jesd204_tx_data_ready` and `jesd204_tx_data_valid` signals are asserted. • The "Short Test Error" is not asserted.
SCR.2	Verify the data transfer from digital to analog domain.	Enable descrambler at the DAC JESD core and scrambler at the TX JESD204B IP core. Enable sine wave generator in the FPGA and observe the DAC analog channel output on the oscilloscope.	A monotone sine wave is observed on the oscilloscope.

Deterministic Latency (Subclass 1)

Figure below shows a block diagram of the deterministic latency test setup. The LMK04828 clock generator provides periodic SYSREF pulses for both the DAC37J84 and JESD204B IP core. The period of SYSREF pulses is configured to 2 Local Multi Frame Clocks (LMFC). The SYSREF pulse restarts the LMF counter and realigns it to the LMFC boundary.

Figure 12: Deterministic Latency Test Setup Block Diagram



The FPGA generates a 16-bit digital sample with a value of 8000 hexadecimal number at the transport layer. The most significant bit of this digital sample has a logic 1 and this bit is pin out at FPGA 1. This bit is transmitted to FPGA 2, which passes this signal to the HSMC breakout board header. This bit is probed at oscilloscope channel 1. The DAC analog channel is probed at oscilloscope channel 2. With two's complement value of 8000h, a pulse with the amplitude of negative full range is expected at DAC analog channel 1. The time difference between the pulses at channel 1 (t0) and channel 2 (t1) is measured. This is the total latency of the JESD204B link, the DAC digital blocks, and analog channel.

Table 5: Deterministic Latency Test Cases

Test Case	Objective	Description	Passing Criteria
DL. 1	Measure the total latency.	Measure the time difference between the rising edge of pulses at oscilloscope channel 1 and 2.	The latency should be consistent.

Test Case	Objective	Description	Passing Criteria
DL. 2	Re-measure the total latency after DAC power cycle and FPGA reconfiguration.	Measure the time difference between the rising edge of pulses at oscilloscope channel 1 and 2.	The latency should be consistent.

JESD204B IP Core and DAC37J84 Configurations

The JESD204B IP core parameters (L, M and F) in this hardware checkout are natively supported by the DAC37J84 device and Quick Start tab of DAC3XJ8XEVM GUI. The transceiver data rate, device clock frequency, and other JESD204B parameters comply with the DAC37J84 operating conditions.

The hardware checkout testing implements the JESD204B IP core with the following parameter configuration.

Table 6: Parameter Configuration

Configuration	Setting	Setting	Setting	Setting
LMF	148	244	442	841
HD	0	0	0	1
S	1	1	1	1
N	16	16	16	16
N’	16	16	16	16
CS	0	0	0	0
CF	0	0	0	0
Subclass	1	1	1	1
DAC Interpolation	8	4	2	1
DAC Device Clock (MHz)	983.04	1228.8	1228.8	1228.8
DAC Data Input Rate (MSPS)	122.88	307.2	614.4	1228.8
FPGA Device Clock (MHz) [6]	245.76	307.2	307.2	307.2

[6] The device clock is used to clock the transceiver.

Configuration	Setting	Setting	Setting	Setting
FPGA Management Clock (MHz)	100	100	100	100
FPGA Frame Clock (MHz) (7)	122.88	307.2	307.2	307.2
FPGA Link Clock (MHz) (7)	245.76	307.2	307.2	307.2
FPGA TX PHY Mode (8)	Bonded	Bonded	Bonded	Non-bonded
PCS Option(9)	Hard PCS	Soft PCS	Soft PCS	Soft PCS
Character Replacement	Enabled	Enabled	Enabled	Enabled
Test Data Pattern	• (0xF1, 0xE2, 0xD3, 0xC4, 0xB5, 0xA6, 0x97, 0x80) (10) • Sine (11) • Single pulse (12)	• (0xF1, 0xE2,0xD3, 0xC4) (10) • Sine (11) • Single pulse (12)	• (0xF1, 0xE2) (10) • Sine (11) • Single pulse (12)	• (0xF1) (10) • Sine (11) • Single pulse (12)

Test Results

The following table contains the possible results and their definition.

Table 7: Results Definition

Result	Definition
PASS	The Device Under Test (DUT) was observed to exhibit conformant behavior.

(7) The FPGA frame clock and link clock for LMF=244, 442, and 841 modes are sourced directly from the FPGA device clock (LMK04828 clock channel CLKout0). For LMF=148 mode, the link clock is sourced directly from the FPGA device clock, while the frame clock is sourced from the LMK04828 clock channel CLKout12 through the FMC connector.

(8) The ATX PLL is used in the JESD204B IP core. The TX PHY mode selected is compatible with the transceiver channel placement rules in the Quartus II software.

(9) A data rate beyond 12200 Mbps requires a soft PCS to be enabled in the JESD204B IP core.

(10) Each frame clock cycle consists of the test pattern in parentheses. Refer to JESD204B specification section 5.1.6.2 for short transport layer test pattern definition.

(11) Sine wave pattern is used in TL.2 and SCR.2 test cases to verify that pattern generated in the FPGA transport layer is transmitted by DAC analog channel.

(12) Single pulse pattern is used in deterministic latency measurement test cases DL.1 and DL.2 only.

Result	Definition
PASS with comments	The DUT was observed to exhibit conformant behavior. However, an additional explanation of the situation is included, such as due to time limitations only a portion of the testing was performed.
FAIL	The DUT was observed to exhibit non-conformant behavior.
Warning	The DUT was observed to exhibit behavior that is not recommended.
Refer to comments	From the observations, a valid pass or fail could not be determined. An additional explanation of the situation is included.

The following table shows the results for test cases CGS.1, CGS.2, ILA.1, ILA.2, ILA.3, TL.1, TL.2, SCR.1 and SCR.2 with different values of L, M, F, SCR, K, data rate, DAC output rate, FPGA link clock and sysref pulse frequency.

Table 8: Test Results

Test	L	M	F	SCR	K	Data rate (Mbps)	DAC Output Rate (MSPS)	FPGA Link Clock (MHz)	Sysref Pulse Frequency (MHz)	Result
1	1	4	8	0	16	9830.4	983.04	245.76	3.84	Pass with comments
2	1	4	8	1	16	9830.4	983.04	245.76	3.84	Pass with comments
3	1	4	8	0	32	9830.4	983.04	245.76	3.84	Pass with comments
4	1	4	8	1	32	9830.4	983.04	245.76	3.84	Pass with comments
5	2	4	4	0	16	12288	1228.8	307.2	9.6	Pass with comments
6	2	4	4	1	16	12288	1228.8	307.2	9.6	Pass with comments
7	2	4	4	0	32	12288	1228.8	307.2	4.8	Pass with comments
8	2	4	4	1	32	12288	1228.8	307.2	4.8	Pass with comments

Test	L	M	F	SCR	K	Data rate (Mbps)	DAC Output Rate (MSPS)	FPGA Link Clock (MHz)	Sysref Pulse Frequency (MHz)	Result
9	4	4	2	0	16	12288	1228.8	307.2	19.2	Pass with comments
10	4	4	2	1	16	12288	1228.8	307.2	19.2	Pass with comments
11	4	4	2	0	32	12288	1228.8	307.2	9.6	Pass with comments
12	4	4	2	1	32	12288	1228.8	307.2	9.6	Pass with comments
13	8	4	1	0	20	12288	1228.8	307.2	20.48	Pass with comments
14	8	4	1	1	20	12288	1228.8	307.2	20.48	Pass with comments
15	8	4	1	0	32	12288	1228.8	307.2	19.2	Pass with comments
16	8	4	1	1	32	12288	1228.8	307.2	19.2	Pass with comments

Table 9: Test Results For Deterministic Latency

Test	L	M	F	SCR	K	RBD (13)	Data rate (Mbps)	DAC Output Rate (MSPS)	FPGA Link Clock (MHz)	Total Latency Result
DL.1	1	4	8	1	32	31	9830.4	983.04	245.76	Pass, ~810.8–811.2 ns
DL.2	1	4	8	1	32	31	9830.4	983.04	245.76	Pass, ~810.9–811.3 ns
DL.1	2	4	4	1	32	31	12288	1228.8	307.2	Pass, ~391.5–391.7 ns
DL.2	2	4	4	1	32	31	12288	1228.8	307.2	Pass, ~391.4–391.6 ns

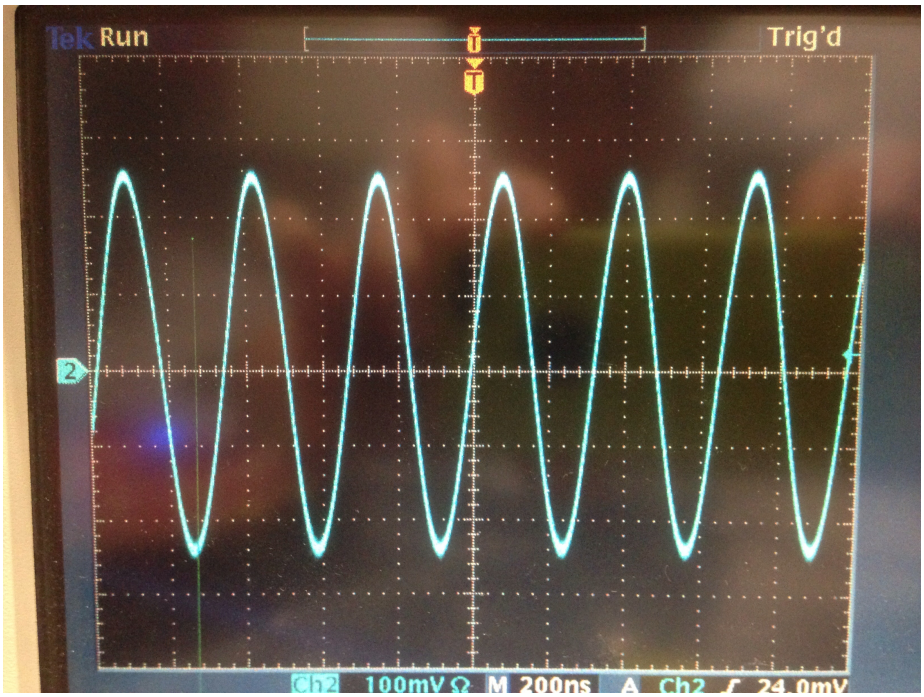
(13) Set the RBD value in the DAC3XJ8XEVM GUI.

Test	L	M	F	SCR	K	RBD (13)	Data rate (Mbps)	DAC Output Rate (MSPS)	FPGA Link Clock (MHz)	Total Latency Result
DL.1	4	4	2	1	32	31	12288	1228.8	307.2	Pass, ~279.1–279.2 ns
DL.2	4	4	2	1	32	31	12288	1228.8	307.2	Pass, ~279.1–279.3 ns
DL.1	8	4	1	1	32	31	12288	1228.8	307.2	Pass, ~215.6–215.8 ns
DL.2	8	4	1	1	32	31	12288	1228.8	307.2	Pass, ~215.6–215.8 ns

Figure 9 shows the results of the alarm and error checking at DAC3XJ8XEVM GUI for LMF = 841 configuration. No link initialization alarm or error is reported.

Figure 13: Sine wave at DAC analog channel output

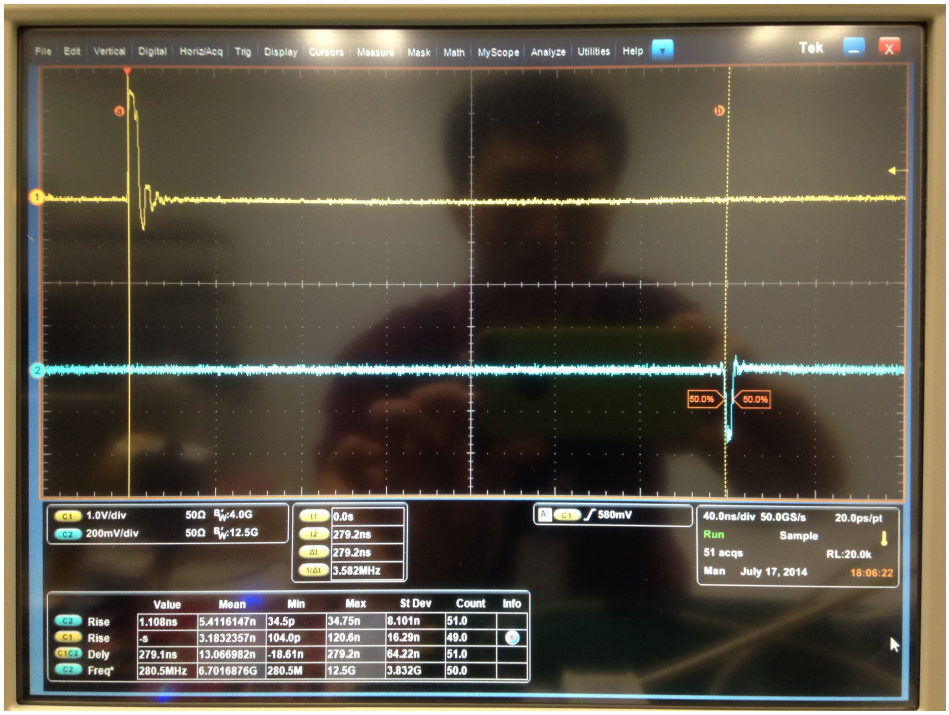
Figure shows the sine wave output from DAC analog channel.



(13) Set the RBD value in the DAC3XJ8XEVM GUI.

Figure 14: Deterministic Latency Measurement For LMF = 442 Configuration

Figure shows the time difference between pulses in deterministic latency measurement for LMF = 442 configuration.



Test Result Comments

In each test case, the TX JESD204B IP core successfully initializes from CGS phase, ILA phase, and until user data phase. The `jesd204_tx_int` signal is asserted because the DAC deasserts `sync_n` initially and then asserts `sync_n` for a duration of more than 5 frames plus 9 octets. The `sync_reinit_req` bit of `tx_err` register (bit 4) is set. Since there is no register available at the DAC to set the initial logic level of `sync_n` signal, the `jesd204_tx_int` signal is asserted during link initialization. There is no other error bit being set in the `tx_err` register throughout CGS.2 and ILAS.1- 3 test cases. Other than the TX interrupt, the behavior of the TX JESD204B IP core meets the passing criteria. To clear the interrupt, write "1" to `tx_err` (bit 4) register. From the **DAC3XJ8X Controls** > **Alarms and Errors** tab in DAC3XJ8XEVM GUI, no error pertaining to RX JESD204B IP core is reported.

For LMF=148 configuration, 9.8304 Gbps is the highest data rate achievable using the EVM on-board clocking mode; the period of SYSREF pulses for K=32 configuration needs to be 1 LMFC in order to get a stable link initialization.

No data integrity issue is observed from the short transport layer test pattern checkers at DAC JESD core. Sine wave is observed at all four analog channels when sine wave generators in FPGA are enabled.

In the deterministic latency measurement, consistent total latency is observed across the JESD204B link and DAC analog channels.

AN 719 Document Revision History

Date	Version	Changes
September 2014	2014.09.22	Revised the deterministic latency measurement results in Table 9.
September 2014	2014.09.05	Initial release.