Understanding JESD204B Subclasses and Deterministic Latency

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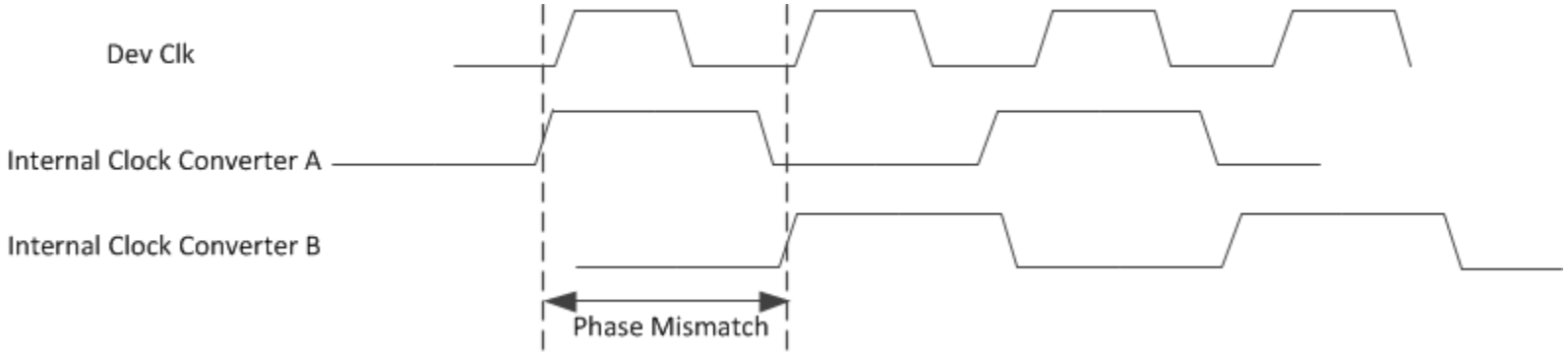
Need for Subclasses – Deterministic Latency

- One of the most desirable features introduced by JESD204B is the deterministic latency of the link between a logic device and multiple data converters.
- As there are various data converters elements in a JESD system working in different clock domains as well as due to such process variations as temperature and supply voltage, latency of the link between transmitter and receiver devices may vary from power up to power up as well as over multiple link reestablishment.
- Unlike JESD204A where an external frame clock input is required to each converter device, JESD204B uses a common device clock going to all the converters which in turn is used to generate internal clocks in each device. Resulting phase mismatch of the divided down clocks in different converter devices causes greatest uncertainty in the link latency.



- The concept of subclasses incepts from different ways to achieve synchronization of the internal clocks across different TX/RX devices. Depending upon a subclass, JESD204B uses SYSREF or SYNC as timing signal for this purpose.

Subclasses

- Subclass 0
  - No support for deterministic latency (backward compatible with JESD204A)
- Subclass 1
  - Deterministic latency achieved using an external ‘SYSREF’ as timing signal
- Subclass 2
  - Deterministic latency achieved using ‘SYNC’ as timing signal

Subclass 0

Subclass 0 does not provide the support for deterministic latency feature of JESD204B. The main objective of subclass 0 is to avail all other features of JESD204B including higher line rates up to 12.5Gbps while still maintaining backward compatibility with JESD204A.

Inter-Device Synchronization

- Subclass 0 may or may not support multiple converter device alignment but always supports multiple lanes alignment within a single device.
- In case of multiple device alignment of different ADC devices, SYNC signal for each lane is combined in the RX logic device and distributed to all ADCs such that all the ADCs see the SYNC falling edge (active low) in the same frame clock period. The clock edge at which SYNC assertion is sampled is used to align the internal clocks across different devices. Note that in such a case frame clock must be whole multiple of the frequency of the device clock and device clock across multiple ADCs must be phase aligned.
- In case of multiple device alignment of different DAC devices, a separate inter-device RX synchronization interface is required to align internal clocks. As per the standard, this interface should be synchronous to the frame clock. Also in case of multiple subclass 0 DACs, SYNC signal from each DAC must be combined and presented as one to the TX so that ILAS generation at TX lanes is synchronized.
- In case of subclass 0, SYNC is a timing critical signal only if multi-device synchronization is desired. In such a case, system must be designed such that SYNC signal going to each ADC must meet setup and hold time with respect to the ADC device clock.

Subclass 0

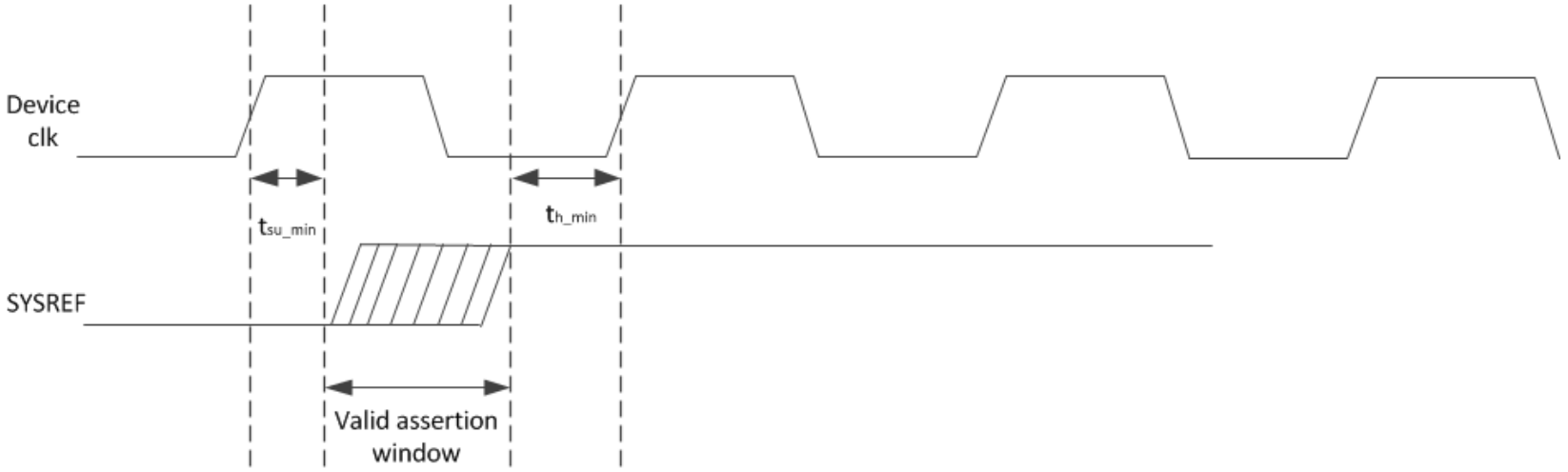
Interoperability with JESD204A

- Subclass 0 is fully backward compatible with JESD204A.
- Similar to JESD204A, in absence of the support for deterministic latency, operations in a subclass 0 device are aligned to frame clock boundary as opposed to the local multiframe clock (LMFC).
- As timing of error reporting using SYNC signal is different between JESD204A and JESD204B, to ensure compatibility, a JESD204B device should allow programming its error reporting/detection to meet the requirements of a JESD204A device.
- It should be ensured that setup/hold time of SYNC signal is not violated at RX otherwise a JESD204B TX can miss the error report from a JESD204A RX or a JESD204A TX can misinterpret error report as a re-synchronization request from a JESD204B RX.
- In case of JESD204B RX working with JESD204A TX, an absence of frame clock input in the RX may result in the violation of SYNC setup/hold time at the TX causing problems in error repotting for errors not requiring re-synchronization as discussed above. Error reporting in such a case can always be disabled (only for errors not requiring resynchronization of the link. See section 7.6 of JESD204B standard for a list of errors) .

Subclass 1

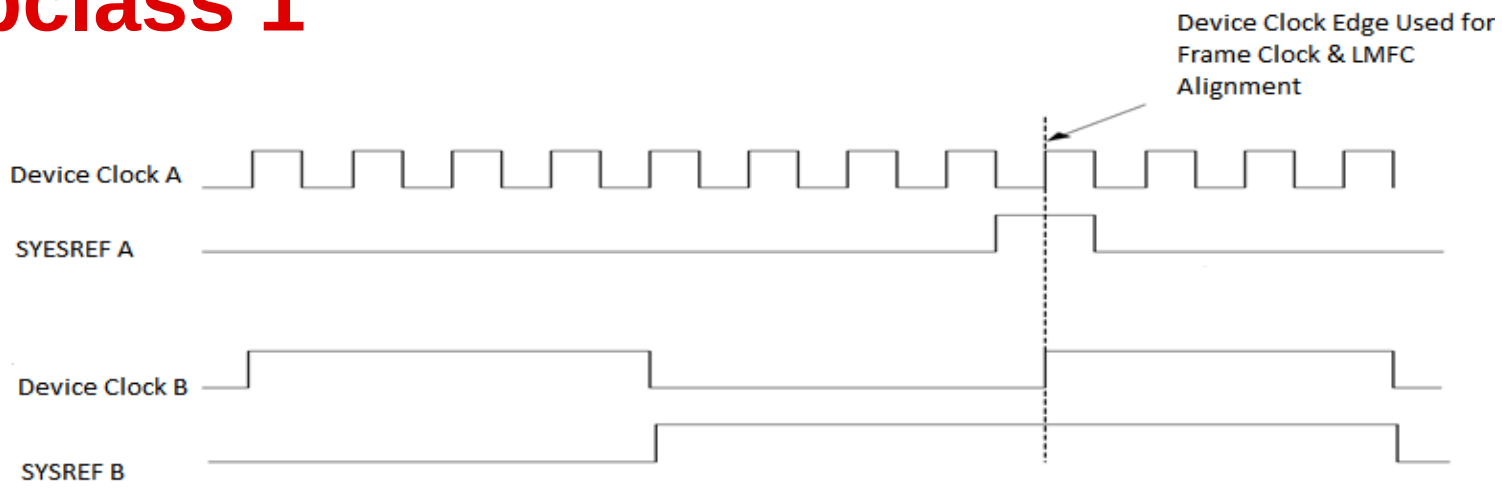
- Subclass 1 uses an external SYSREF signal to act as a common timing reference for multiple devices in a JESD204B system to achieve deterministic latency. SYSREF is source synchronous to the device clock.
- SYSREF can be a one-shot, gapped periodic or a periodic signal. Incase of periodic or gapped periodic, period of the SYSREF must be integer multiple of the Local Multi Frame Clock (LMFC) in order to avoid SYSREF pulse in the middle of a multiframe.
- Synchronization across multiple TX/RX devices is achieved by having phase aligned device clocks across all the devices and making SYSREF synchronous to the device clock. The internal frame and LMFC clocks within each TX/RX device are aligned to that edge of the device clock where SYSREF is sampled high. This in turn also aligns the internal clocks of all the devices (TX or RX) with each other.
- For correct alignment, SYSREF should meet setup and hold time of the device clock and must be distributed to each TX/RX device with matched trace length and signal type relative to the device clock. TX/RX device should specify the setup and hold time requirements of SYSREF with respect to the device clock at the input.

Subclass 1



- In order for the internal clocks be aligned across multiple devices, skew between the device clock pins should be minimized and SYSREF be generated from the same clock generator used for generating TX/RX device clock.
- As per standard, it is not mandatory to generate same SYSREF for all the TX/RX devices. However, SYSREF must be generated for all the devices such that there is a deterministic relationship between when SYSREF is sampled high in all the devices, as shown below in the standard.

Subclass 1



- Once alignment is completed, future SYSREF pulses may be used to check the alignment of the local frame and multiframe clocks.
- Since a periodic SYSREEF signal acts as a sub-harmonic clock of the converter sampling clock and may have spurious effect on the converter performance, it may be turned off during normal operation once synchronization has been achieved.
- If SYSREF is turned off during normal operation, TX and RX devices must have the ability to generate a “Generate SYSREF” request to the clock generator whenever a synchronization request is detected at the SYNC interface.

Subclass 1

Deterministic Latency Procedure

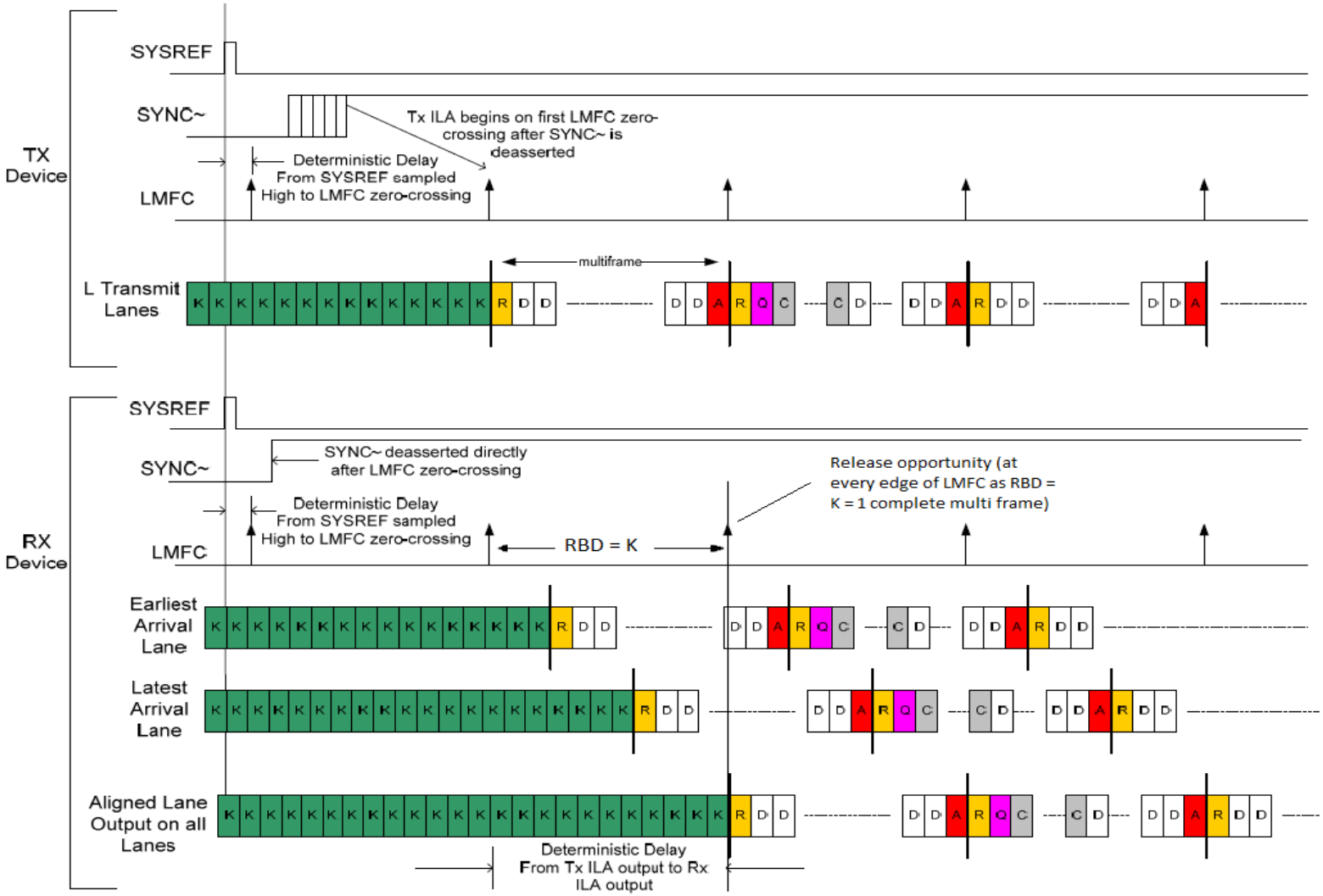
- As mentioned before, Deterministic latency in subclass 1 devices is achieved using the SYSREF signal.
- Since SYSREF aligns all the LMFCs, Initial Lane Alignment Sequence (ILAS) is generated simultaneously on all lanes at an LMFC boundary (after SYNC signal is asserted indicating code group synchronization).
- RX buffers the incoming data on all lanes in order to account for the skew on TX/RX SERDES and the physical channels.
- The data is output from the buffers at the same time when there is a valid data in receiver elastic buffer of all lanes and a ‘release opportunity’ present.
- Valid data is the start of ILAS or start of user data (if ILAS is not buffered) .The release opportunity occurs after a fixed number of frame cycles, called Receiver Buffer Delay (RBD), following an LMFC boundary. RBD ranges from 1 to K (K is no. of frames in a multiframe) (see figure in the next slide).
- The above sequence of operations cause latency between when parallel frame based ILAS data is generated in TX and when it is released at the output of RX buffers to be a known repeatable value. As can be seen, this relies on the correct alignment of LMFCs within TX and RX devices.

Subclass 1

Deterministic Latency Procedure (cont'd)

- The size of RX elastic buffer (per lane) must be large enough to store all the data arrived between the earliest possible instant of data arrival on RX buffer input to the next release opportunity.
- Also value of RBD must be chosen such that data for all lanes arrive in the buffers before the next release opportunity (applicable if RBD value less than K is to be chosen to minimize latency).
- Figure in the next slide, as shown in the JESD204B standard, presents a graphical view of deterministic latency procedure for subclass 1 devices. Note that in this example, receiver buffer delay has been set to K so that the release opportunity occurs at every LMFC edge.
- The value of RBD can be chosen to be less than K as well in order to minimize latency. Refer to the standard for the requirements on RBD value.

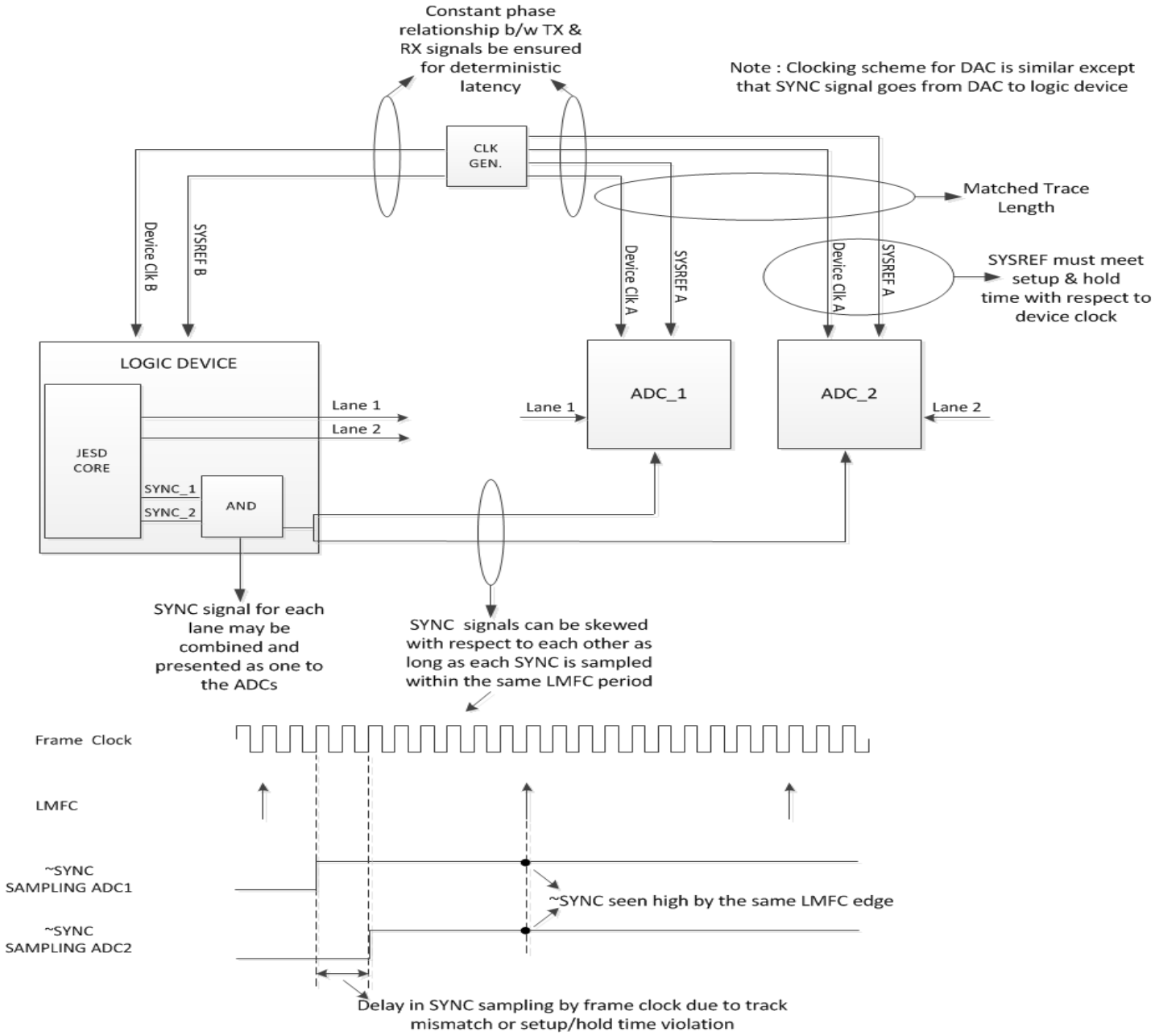
Deterministic Latency



Subclass 1

Deterministic Latency Procedure (cont'd)

- To summarize, in order to minimize uncertainty in the latency for subclass 1, following steps must be taken:
  - Device clocks of all the converter devices must be aligned.
  - SYSREF to each device must be distributed such that the device edge sampling SYSREF high is aligned in all devices.
  - SYSREF period(if periodic) must be multiple of LMFC period.
  - Although LMFCs between TX and RX need not to be aligned, there must be a constant phase relationship between them. Any variation in the phases of the two LMFCs would result in the variation of link latency. As per standard, device must specify a deterministic delay between when SYREF is sampled high and the rising edge of the LMFC after phase reset as shown in the figure in previous slide. Hence a constant phase relationship between TX and RX SYSREF (and device clock) would result in a constant phase between LMFC of TX and RX. See Latency Variation section at the end of document.
  - Figure in the next slide shows the clocking scheme and timing signals for subclass 1 devices.


Constant phase relationship b/w TX & RX signals be ensured for deterministic latency
Note : Clocking scheme for DAC is similar except that SYNC signal goes from DAC to logic device
CLK GEN.
Matched Trace Length
Device Clk B
SYSREF B
Device Clk A
SYSREF A
Device Clk A
SYSREF A
SYSREF must meet setup & hold time with respect to device clock
LOGIC DEVICE
JESD CORE
SYNC_1
SYNC_2
AND
Lane 1
Lane 2
Lane 1
ADC_1
ADC_2
Lane 2
SYNC signal for each lane may be combined and presented as one to the ADCs
SYNC signals can be skewed with respect to each other as long as each SYNC is sampled within the same LMFC period
Frame Clock
LMFC
~SYNC SAMPLING ADC1
~SYNC SAMPLING ADC2
~SYNC seen high by the same LMFC edge
Delay in SYNC sampling by frame clock due to track mismatch or setup/hold time violation

Subclass 2

- Subclass 2 uses the active low SYNC signal to act as a common timing reference for multiple devices in a JESD204B system to achieve deterministic latency.
- Following the reception of four successive K28.5 comma symbols, receiver asserts the SYNC signal (high to low) at the frame clock edge corresponding to an LMFC boundary.
- On the TX side, SYNC assertion is sampled by a high speed detection clock (usually frame or device clock, whichever is faster).

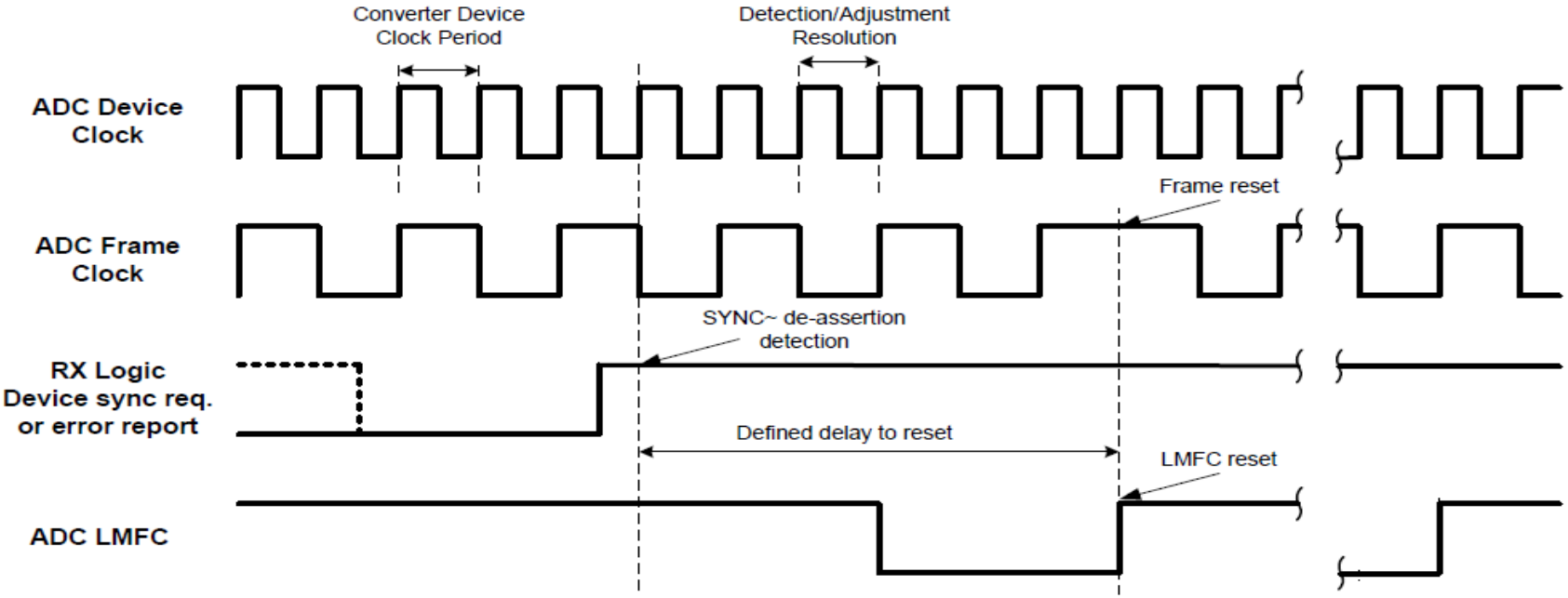
LMFC Phase Adjustment – ADC

- In the case of ADC, the edge which samples the SYNC assertion is used to align frame clock and LMFC. For this purpose an adjustment clock is used which defines the adjustment resolution of the LMFC and frame clock. The adjustment clock frequency is set equal to the fastest frequency in the link which can either be the device clock of TX or RX.

Subclass 2

LMFC Phase Adjustment – ADC (cont'd)

- Figure below shows timing diagram to adjust phase of LMFC and frame clock as given in the JESD204B standard. The device clock edge sampling ~SYNC high serves as the alignment reference. Since all device clocks are aligned across different converters, this aligns all the internal clocks of different ADCs provided SYNC is sampled at the same device edge. Note that as per standard, there must be a known delay between when ~SYNC is sampled high to when phases of internal clocks are reset. This delay for a specific device must be constant to avoid uncertainty in the latency.



Subclass 2

LMFC Phase Adjustment – DAC

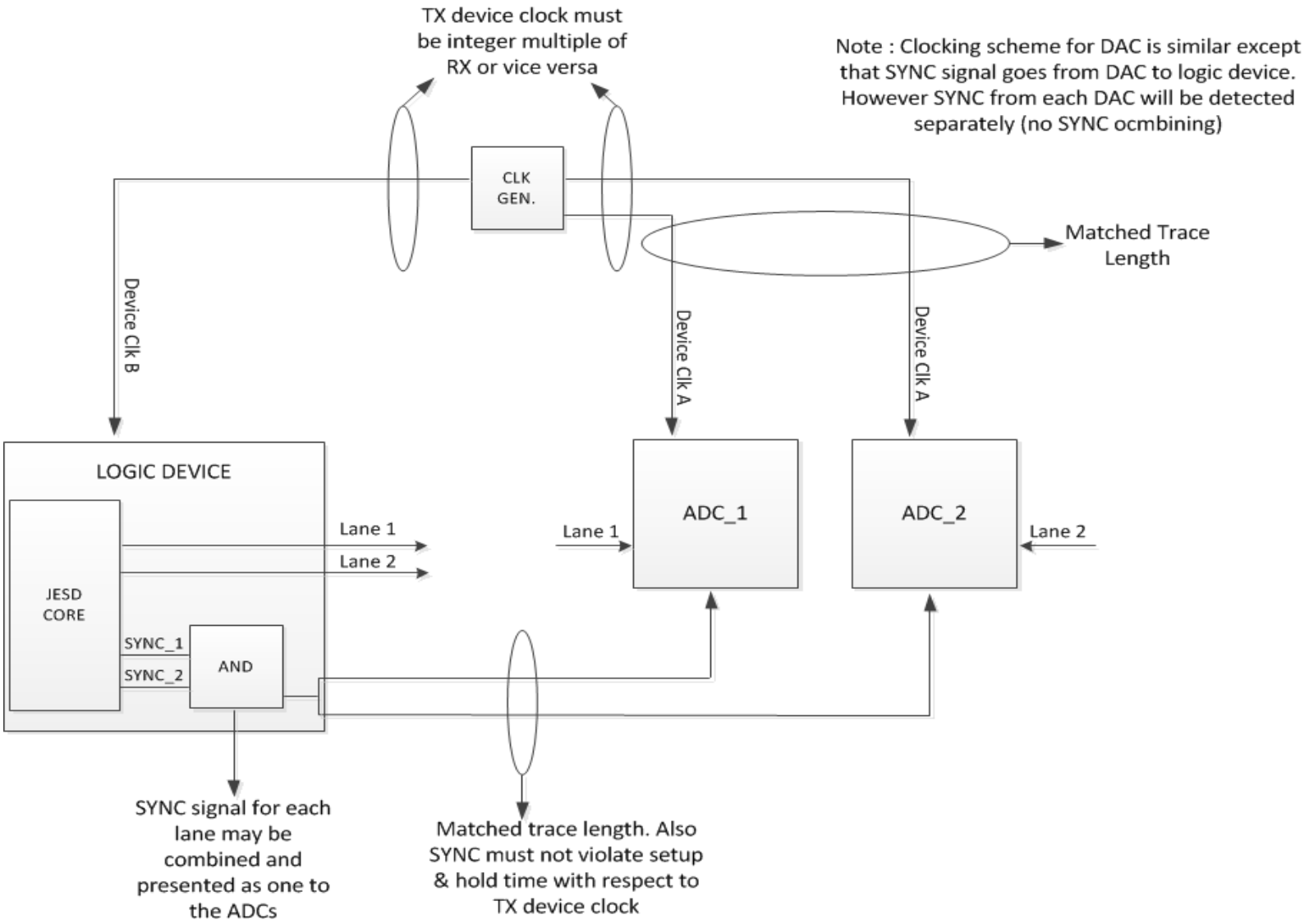
- One power up, for a multipoint link, LMFC of different DACs may be misaligned with respect to each other causing uncertainty in the latency.
- LMFC of each DAC is aligned with respect to LMFC of the logic device since it is common in the JESD204B link (as there is only one logic device).
- Assertion of SYNC signal from each DAC is detected by a detection clock in the logic device similar to ADC.
- TX computes the misalignment between the edge sampling SYNC assertion and rising edge of it own LMFC for each SYNC signal.
- If there is a misalignment, the information is embedded within the link configuration data sent in the second multiframe of ILAS. Following parameters are used to send the phase adjustment information
  - PHADJ : This is a 1-bit signal asserted if DAC LMFC phase adjustment is needed
  - ADJCNT : Number of adjustment resolution steps to adjust DAC LMFC (in units of DAC adjustment resolution. TX must know adjustment resolution of DAC)
  - ADJDIR : Direction of phase adjustment, 0 – Advance ; 1 – Delay
- As SYNC signal from each DAC carries phase information of its LMFC, the skew in different SYNC signals at TX input pins due to propagation delay (track mismatch) must be minimized.

Subclass 2

Deterministic Latency Procedure

- Deterministic latency procedure for subclass 2 ensues same sequence of events as for subclass 1 except that LMFCs across different converters are aligned using SYNC as the timing signal as discussed earlier.
- As opposed to SYSREF being a source synchronous signal in subclass 1, SYNC is a system synchronous signal. This implies that system must be designed in such a way that SYNC does not violate setup and hold time of TX device clock when it reaches TX input otherwise LMFCs across converters can be misaligned.
- Since meeting setup and hold time becomes a challenge at higher sampling rates, it is recommended, as per standard, to use Subclass 1 for speeds above 500MSPS for both ADC and DAC.

Clocking Scheme - Subclass 2



Summary

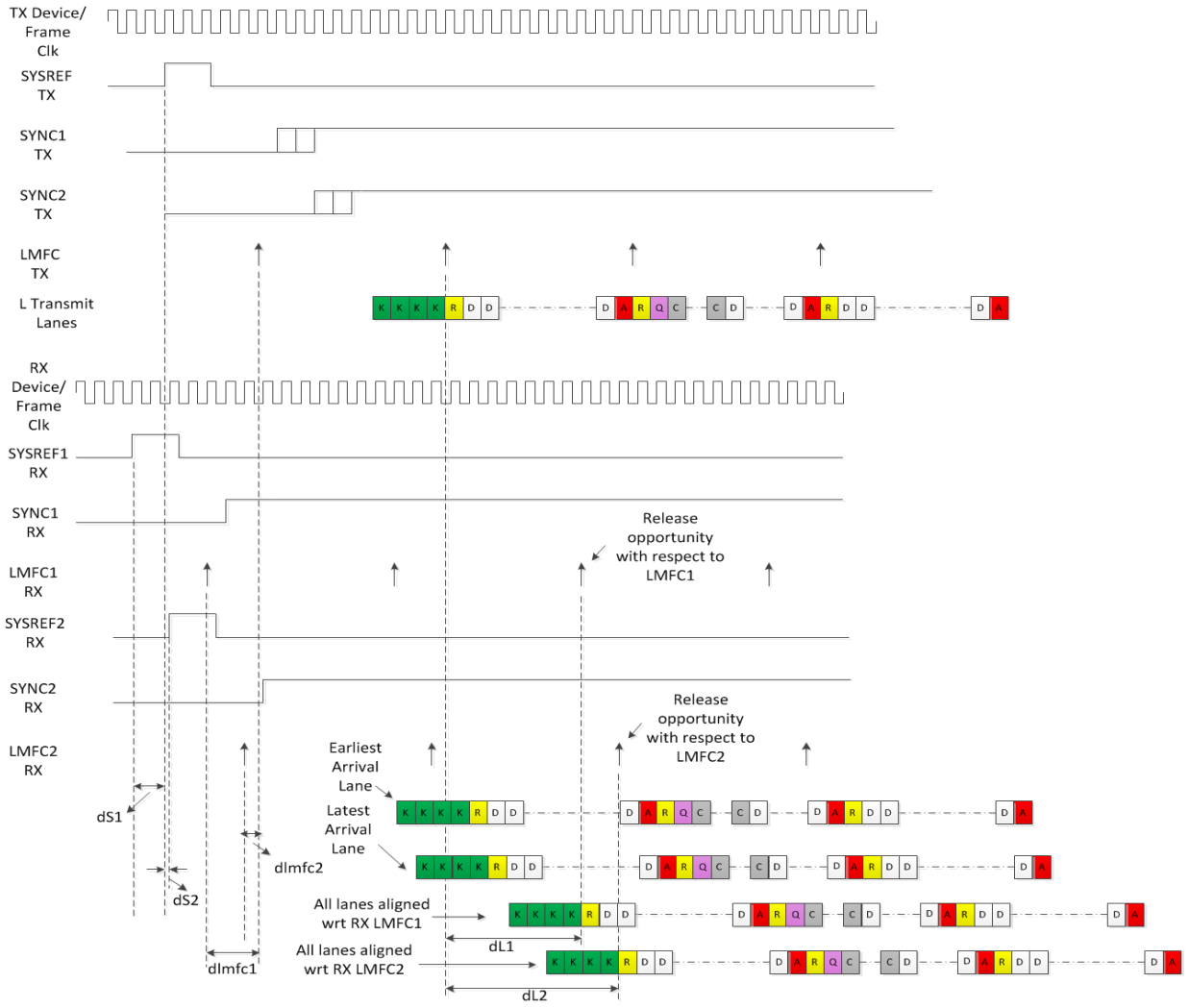
This table highlights important differences between different subclasses of JESD204B standard :

Subclasses	Det. Latency	Timing Signal	SYNC Assertion & Data Transmission	Multiple Converters Alignment	JESD20A Compatibility	Relation Between LMFC & Device Clock	Relation Between TX & RX Device Clock
0	No	SYNC	Frame Clock Boundary	Optional	Yes	N/A	Implementation Dependent
1	Yes	SYSREF	Frame + LMFC clock boundary	Must	No	LMFC period is integer multiple of Device Clock Period	Implementation Dependent
2	Yes	SYNC	Frame + LMFC clock boundary	Must	No	LMFC period is integer multiple of Device Clock Period	TX device clock must be integer multiple of RX device clock or vice versa

Latency Variation - Informative

- This is an informative section describing how the change in the relative phases of TX and RX LMFCs cause variation in the link latency as shown in the figure on next the page. The timing diagram has been drawn for subclass 1 however a similar argument is applied for subclass 2 operation except that SYNC acts as timing signal to align LMFCs.
- In subclass 1, SYSREF acts as a timing signal and the edge of the device clock at which SYSREF is sampled high is used to align LMFCs across different converter devices. As per the standard, delay between SYSREF sampled high and phase reset of LMFC should be constant for the device.
- Figure shows ‘SYSREF TX’ signal which resets the phase of internal clocks in the transmitter and generate ‘LMFC TX’ edge. Similarly ‘SYSREF1 RX’ signal which resets the phase in the receiver and generates ‘LMFC1 RX’. The relative phase difference between the LMFC TX and LMFC1 RX is marked as ‘dlmfc1’. The resulting link latency is marked as ‘dL1’.
- ‘SYSREF2 RX’ shows a shifted version of SYSREF1 RX. The relative phase difference between LMFC TX and ‘LMFC2 RX’ (receiver LMFC generated with respect to SYSREF2 RX) is ‘dlmfc2’ and the resulting link latency is ‘dL2’.
- As can be seen, as the relative phase difference between LMFCs of TX and RX changes (dlmfc1-dlmfc2), it results in the variation of latency (dL2-dL1). Therefore it is necessary to maintain a constant phase relationship between the LMFCs of TX and RX to avoid change in the link latency.
- As can be noted from the figure, in order to maintain a constant phase relationship between TX and RX LMFC, SYSREF of TX and RX should be launched with a constant delay with respect to each other every time synchronization is required.
- A similar variation in the latency will occur if instead of SYSREF, there is a change in the phases between TX and RX device clocks. Therefore, in order to minimize uncertainty in the link latency, there should always be a constant relationship between the TX device clock/sysref and RX device clock/sysref.

Latency Variation - Informative



Latency Variation Due to Variation between TX and RX LMFCs phase

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