# Sipeed M1 Datasheet

# v1.1



## Key Features：

- CPU : RISC-V Dual Core 64bit, with FPU，400Mhz-500Mhz, Neural network processor
- Image Recognition: QVGA@60FPS/VGA@30FPS
- Voice Recognition: up to 8 microphones
- Deep learning framework: TensorFlow/Keras/Darknet
- Peripheral: FPIOA、UART、GPIO、SPI、I²C、I²S、WDT、TIMER、RTC etc.

| UPDATE | |
|---|---|
| V1.0 | 2018/10/25 Published original document |
| V1.1 | 2019/3/6：Removed M1w description |
| | |

| SPECIFICATION | |
|---|---|
| CPU : RISC-V Dual Core 64bit, 400Mh adjustable | Powerful dual-core 64-bit open architecture-based processor with rich community resources |
| FPU Specifications | IEEE754-2008 compliant high-performance pipelined FPU |
| Debugging Support | High-speed UART and JTAG interface for debugging |
| Neural Network Processor (KPU) | • Supports the fixed-point model that the mainstream training framework trains according to specific restriction rules<br>• There is no direct limit on the number of network layers, and each layer of convolutional neural network parameters can be configured separately, including the number of input and output channels, and the input and output line width and column height<br>• Support for 1x1 and 3x3 convolution kernels<br>• Support for any form of activation function<br>• The maximum supported neural network parameter size for real-time work is 5MiB to 5.9MiB<br>• The maximum supported network parameter size when working in non-real time is (flash size - software size) |
| Audio Processor (APU) | • Up to 8 channels of audio input data, ie 4 stereo channels<br>• Simultaneous scanning pre-processing and beamforming for sound sources in up to 16 directions<br>• Supports one active voice stream output<br>• 16-bit wide internal audio signal processing<br>• Support for 12-bit, 16-bit, 24-bit, and 32-bit input data widths • Multi-channel direct raw signal output<br>• Up to 192kHz sample rate<br>• Built-in FFT unit supports 512-point FFT of audio data<br>• Uses system DMAC to store output data in system memory |
| Static Random-Access Memory (SRAM) | The SRAM is split into two parts, 6MiB of on-chip general-purpose SRAM memory and 2MiB of on-chip AI SRAM memory, for a total of 8MiB |
| Field Programmable IO Array (FPIOA/IOMUX) | FPIOA allows users to map 255 internal functions to 48 free IOs on the chip |
| Digital Video Port (DVP) | Maximum frame size 640x480 |

| FFT Accelerator | The FFT accelerator is a hardware implementation of the Fast Fourier Transform (FFT) |
|---|---|

## SOFTWARE FEATURES

| FreeRtos & Standard SDK | Support FreeRtos and Standrad development kit. |
|---|---|
| MicroPython Support | Support MicroPython on M1 |
| Machine vision | Machine vision based on convolutional neural network |
| Machine hearing | High performance microphone array processor |

## HARDWARE FEATURES

| Supply voltage of external power supply | 5.0V ±0.2V |
|---|---|
| Supply current of external power supply | > 300mA @ 5V |
| Temperature rise | <30K |
| Range of working temperature | -30℃ ~ 85℃ |

## M1 PIN MAP
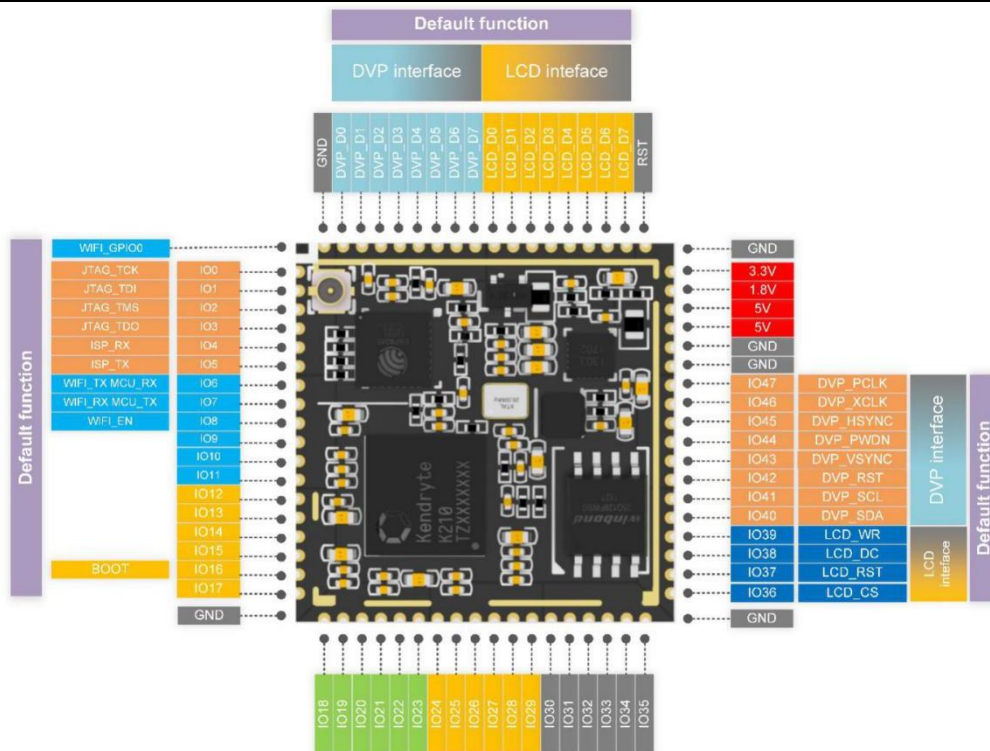
## M1 BLOCK DIAGRAM
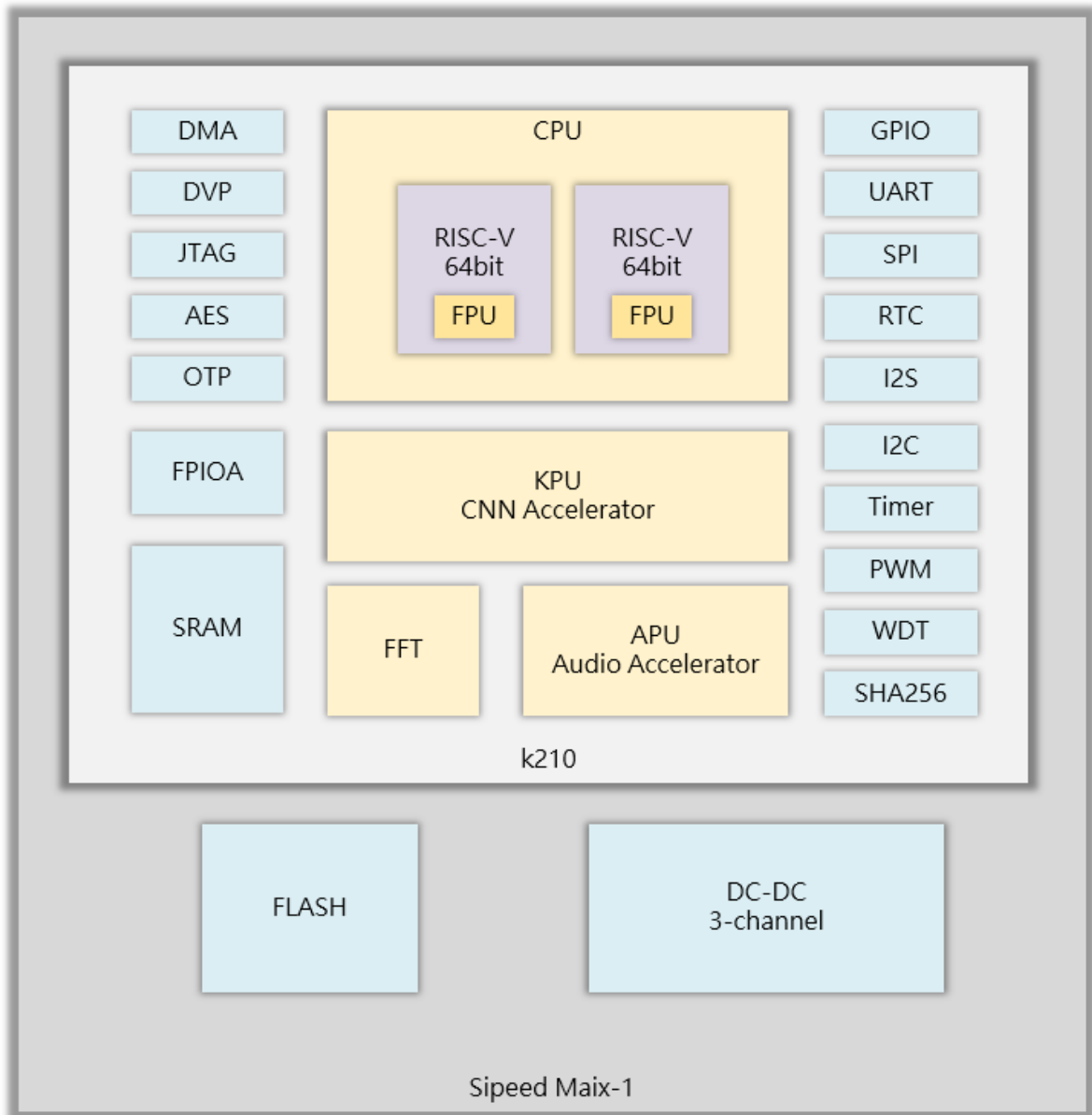
| SIZE | |
|---|---|
| Length | 25.4mm |
| Width | 25.4mm |
| Height | 3.3 mm |

## Sipeed M1 PIN ASSIGNMENT
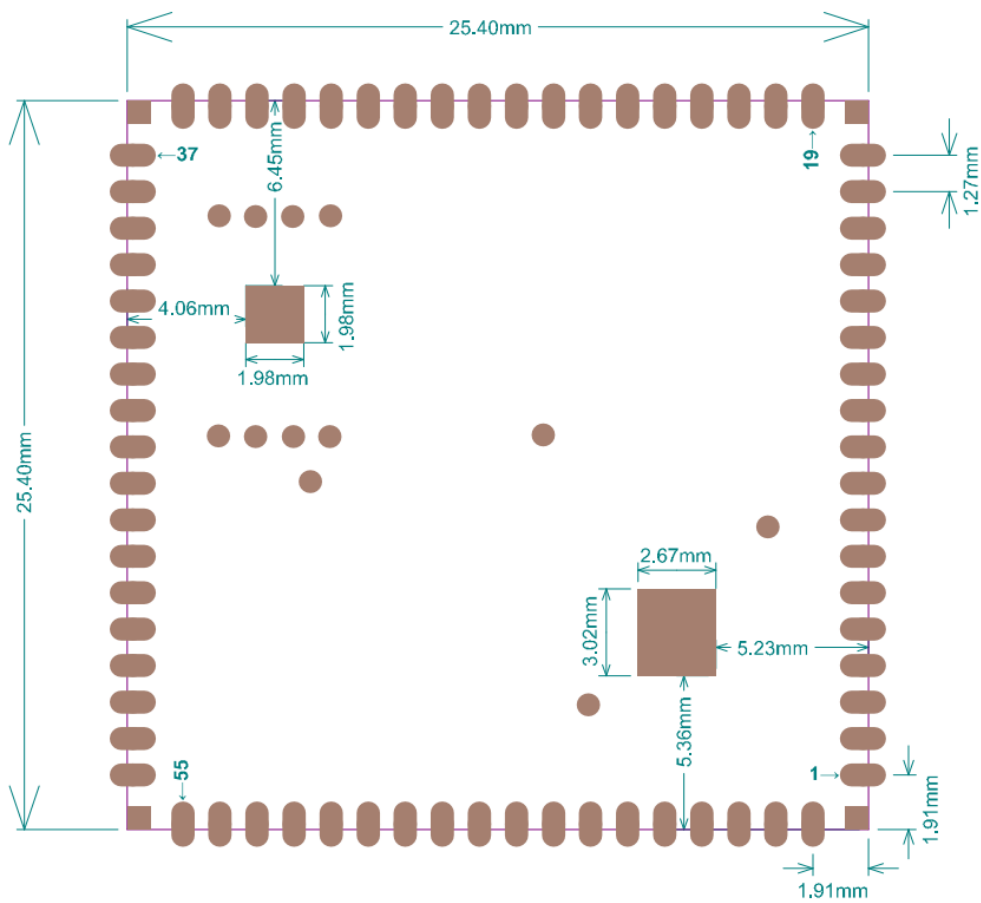
| # | PIN | # | PIN | # | PIN | # | PIN |
|---|-----|---|-----|---|-----|---|-----|
| 1 | JTAG_TCK | 19 | MIC_BCK | 37 | LCD_CS | 55 | RST |
| 2 | JTAG_TDI | 20 | MIC_WS | 38 | LCD_RST | 56 | LCD_D7 |
| 3 | JTAG_TMS | 21 | MIC_DAT3 | 39 | LCD_DC | 57 | LCD_D6 |
| 4 | JTAG_TDO | 22 | MIC_DAT2 | 40 | LCD_WR | 58 | LCD_D5 |
| 5 | ISP_RX | 23 | MIC_DAT1 | 41 | DVP_SDA | 59 | LCD_D4 |
| 6 | ISP_TX | 24 | MIC_DAT0 | 42 | DVP_SCL | 60 | LCD_D3 |
| 7 | WIFI_TX MCU_RX | 25 | MIC_LED_DAT | 43 | DVP_RST | 61 | LCD_D2 |
| 8 | WIFI_RX MCU_TX | 26 | SPI0_CS1 | 44 | DVP_VSYNC | 62 | LCD_D1 |
| 9 | WIFI_EN | 27 | SPI0_MISO | 45 | DVP_PWDN | 63 | LCD_D0 |
| 10 | IO9 | 28 | SPI0_SCLK | 46 | DVP_HSYNC | 64 | DVP_D7 |
| 11 | IO10 | 29 | SPI0_MOSI | 47 | DVP_XCLK | 65 | DVP_D6 |
| 12 | IO11 | 30 | SPI0_CS0 | 48 | DVP_PCLK | 66 | DVP_D5 |
| 13 | LED_G | 31 | MIC0_WS | 49 | GND | 67 | DVP_D4 |
| 14 | LED_B | 32 | MIC0_DATA | 50 | GND | 68 | DVP_D3 |
| 15 | LED_R | 33 | MIC0_BCK | 51 | 5V | 69 | DVP_D2 |
| 16 | IO15 | 34 | I2S_WS | 52 | 5V | 70 | DVP_D1 |
| 17 | BOOT KEY0 | 35 | I2S_DA | 53 | 1V8 | 71 | DVP_D0 |
| 18 | IO17 | 36 | I2S_BCK | 54 | 3V3 | 72 | GND |

Note: The small square pad in the lower right corner of the dimension drawing is WIFI_GPIO0, and the other three corners are GND.

## REFLOW PROFILE GUIDELINE
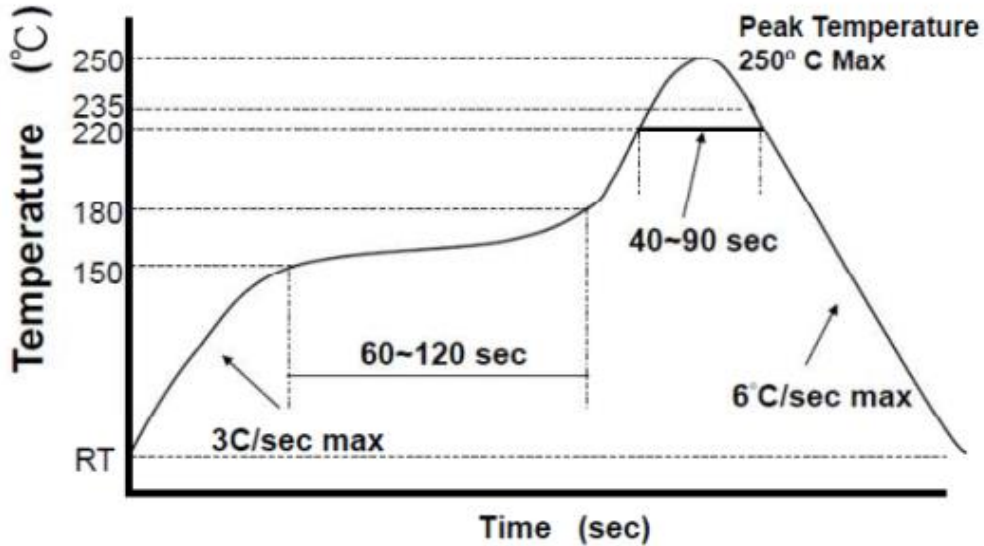


## Matters needing attention

| | |
|---|---|
| Boot mode selection | At startup, BOOT pin is used to select one of two boot options:<br>● Boot from main flash memory (Set BOOT pin 3.3V)(Float or pull up to 3.3V)<br>● Enter ISP download mode (Set BOOT pin 0V) |
| RST pin | Vrst range : 0 to 1.8V ; Active low ; Do not let the voltage of RST pin be greater than 1.8V |
| Thermal design | It is recommended to connect the pad on the bottom of the module to a large piece of copper on the bottom plate to help heat dissipation |
| | |

| RESOURCES | |
|---|---|
| Official Website | www.sipeed.com |
| Github | https://github.com/sipeed |
| BBS | http://bbs.sipeed.com |
| Wiki | maixpy.sipeed.com |
| Sipeed Model Store | https://maixhub.com/ |
| SDK Reference | dl.sipeed.com/MAIX/SDK |
| HDK Reference | dl.sipeed.com/MAIX/HDK |
| E-mail (Technical Support) | support@sipeed.com |
| Telegram Link | https://t.me/sipeed |
| QQ Group | 878189804 |

### Disclaimer and copyright notice

The information in this document, including the URL address for reference, is subject to change without notice.

The documentation is provided by Sipeed without warranty of any kind, including any warranties of merchantability, and any proposal, specification or sample referred to elsewhere. This document is not intended to be a liability, including the use of information in this document to infringe any patent rights.